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Martin Estorninho Blocher

Solid-State Transformer Application For a Grid-Connected Energy Storage System

VOLUME 1

Dissertation in the context of the Master in Electrical and Computer Engineering, Specialization in Energy, advised by Professor Doctor André Mendes and presented to the Department of Electrical and Computer Engineering at the Faculty of Sciences and Technology of the University of Coimbra.

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Abstract

The energy sector is undergoing a major change as global warming urges governments to react. This implies shifting the existing electrical infrastructure toward decentralized power generation while increasing the share of Renewable Energy Sources (RES). This transition requires the implementation and development of new technologies capable of integrating Distrusted Energy Sources (DES), while maintaining the overall Power Quality (PQ) of the system. The Solid-State Transformer (SST) is an emerging technology that will gradually replace the classical Low-Frequency Transformer (LFT) once it can integrate DES and provide needed ancillary services to the electrical grid. This dissertation presents the study of a bidirectional SST application to integrate a Battery Storage System (BSS) into the high voltage electrical grid. For this a two-stage conversion SST was developed. The Modular Multilevel Converter (MMC) with a Model Predictive Control (MPC) algorithm was selected for the first stage's design due to its modularity and scalability while maintaining the system's PQ. The Dual Active Bridge (DAB) converter with Phase Shift Modulation Control was elected for the second stage, connecting the BSS to the first conversion stage while providing galvanic isolation to the system. The MMC characteristics were the primary focus of this research. These characteristics included several control objectives, such as circulating current minimization and submodule voltage balancing, as well as the converter's ability to cope with system fluctuations such as grid voltage disturbances or component parameter variations. In this work, a brief State of the Art of SST technology is presented, followed by the system's complete configuration, modelling, and control system. Finally, a simulation in a Matlab/Simulink environment is undertaken to validate the research made. The results reveal that the system is capable of charging and discharging the BSS at varying rates while maintaining an adequate overall system PQ.

Keywords— Power Distribution, Solid-State Transformer, Power Electronics, Modular Multilevel Converter, Energy Storage Systems.

Resumo

O setor energético está a sofrer uma mudança significativa à medida que o aquecimento global pressiona os governos a atuarem. Em consequência, na infraestrutura da rede elétrica existente, observa-se uma transição para uma geração mais descentralizada aumentando assim a percentagem de fontes de energia renováveis. Esta requer a implementação e desenvolvimento de novas tecnologias capazes de integrar fontes de energia distribuídas, mantendo em simultâneo a qualidade de potência na rede. O transformador de estado sólido é uma tecnologia emergente que irá gradualmente substituir o transformador de baixa frequência, já que consegue integrar este tipo de fontes de energia e fornecer serviços auxiliares à rede necessários para manter a sua qualidade de potência. Esta dissertação apresenta o estudo de um transformador de estado sólido bidirecional para a integração de um sistema de baterias à rede elétrica. Assim, desenvolveu-se um transformador de estado sólido com dois estágios de conversão e foi eleito o conversor multinível modular com uma estratégia de controlo de modelo preditivo para o primeiro estágio, devido à sua modularidade e escalabilidade, garantindo a qualidade de potência do sistema. Para a ligação do sistema de baterias ao primeiro estágio optou-se pelo conversor DC-DC de dupla ponte ativa, já que este fornece isolamento galvânico ao sistema. O conversor modular de multinível foi o principal foco deste estudo com uma análise profunda sobre as suas características. Vários objetivos de controlo como a minimização das correntes circulantes e o equilíbrio das tensões dos seus submódulos foram analisados, bem como a capacidade do conversor em lidar com flutuações, tais como perturbações nas tensões da rede ou variações dos parâmetros dos seus componentes. Esta dissertação inicia-se com um breve estado da arte deste tipo de transformadores, seguida da configuração, modelização e estratégia de controlo para o sistema desenvolvido. Finalmente, os resultados obtidos através de uma simulação em ambiente Matlab/Simulink são discutidos, de forma a validar este estudo. Estes vão demonstrar que o sistema é capaz de carregar e descarregar o sistema de baterias a vários níveis, não afetando a qualidade de potência ao longo do sistema.

Palavras-Chave— Distribuição de Potência, Transformador de Estado Sólido, Eletrónica de Potência, Conversor Modular de Multinível, Sistemas de Armazenamento de Energia.

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List of Abbreviations

AC Alternating Current.

BSS Battery Storage System.

CC Circulating Current.

CMV Common-Mode Voltage.

DAB Dual-Active Bridge.

DC Direct Current.

DES Distributed Energy Sources.

ESS Energy Storage Systems.

HB-SM Half-Bridge Submodule.

HF High-Frequency.

HFT High-Frequency Transformer.

HV High-Voltage.

IPOP Input Parallel Output Parallel.

IRENA International Renewable Energy Agency.

ISOP Input Series Output Parallel.

ISOS Input Series Output Series.

LFT Low-Frequency Transformer.

LV Low-Voltage.

MMC Modular Multilevel Converter.

MPC Model Predictive Control.

MV Medium-Voltage.

OSS Optimal Switching State.

OSV Optimal Switching Vector.

OVL Optimal Voltage Level.

PI Proportional-Integral.

PLL Phase-Locked-Loop.

PQ Power Quality.

PWM Pulse-Width Modulation.

RES Renewable Energy Sources.

SiC Silicon Carbide.

SM Submodule.

SOC State of Charge.

SPS Single-Phase Shift.

SST Solid-State Transformer.

THD Total Harmonic Distortion.

ZVS Zero Voltage Switching.

Nomenclature

V_g	Rated grid phase voltage
V_{ll}	Rated grid line-to-line voltage
V_{DC-1}	DC-Link-1 voltage
V_{DC-2}	DC-Link-2 voltage
i_{DC-1}	DC-Link-1 current
i_{DC-2}	DC-Link-2 current
N	Number of SMs used in all MMC arms
n	Grid source common point
o	DC-Link-1 midpoint
L_m	MMC arm inductor
r_m	MMC arm inductor resistance
L_d	DC-Link-1 cable inductance

L_r	DC-Link-1 cable resistance
L_f	Grid filter inductor
r_f	Grid filter inductor resistance
$quantity^m$	Measured quantity
$quantity^p$	Predicted quantity
T_{sc}	MMC controller sampling time
r	Control Variable
r^*	Control Variable Reference
$x \in \{u, l\}$	MMC upper(u)/lower(l) arm
$y \in \{a, b, c\}$	MMC/Grid phase
$h \in \{1...N\}$	Number of SMs in one MMC arm
V_{xy}	MMC arm voltages
i_{xy}	MMC arm currents
i_{zy}	MMC circulating currents
i_{gy}	Grid Phase currents
V_{no}	MMC CMV term
V_{cxyh}	HB-SM capacitor voltage
i_{cxyh}	HB-SM capacitor current
V_{SM}	SM capacitor voltage
S_{xyh}	MMC HB-SM optimal switching state
G_{xy}	MMC Arm voltage level
G_t	MMC voltage vector
f_1	MPC Stage-I cost function
λ_0	Grid current weighting factor used in f_1
λ_1	Circulating currents weighting factor used in f_1
f_2	MPC Stage-II cost function
λ_v	SM capacitors voltage weighting factor used in f_2

M_{1-8}	DAB converter MOSFETS
N_{DAB}	Number of DABs used in the second conversion stage
L_{DAB}	DAB external energy transfer inductor
L_k	DAB equivalent inductance
V_1	DAB HVDC-Link rated voltage
V_2	DAB LVDC-Link rated voltage
$V_{AC-1/2}$	Squarewave voltages applied to the HFT's terminals
f_d	DAB switching frequency
T_d	DAB switching cycle
V_l	Voltage across L_k
i_l	Current flowing through L_k
φ	Phase Shift between V_{AC-1} and V_{AC-1}
T_{1-2}	BSS DC-DC converter MOSFETS
V_{BAT}	Battery Pack voltage
i_{BAT}	Battery Pack current
L_{BAT}	Battery Pack filter inductor

Contents

Chapter 1

Introduction

1.1 Context and Motivation

Power generation, distribution and transmission are the three main stages of the power system in which transformers play an essential role. The traditional Low-Frequency Transformer (LFT) is a rigid, reliable and long-life expectancy (more than 35 years [25]) machine that can handle harsh environmental conditions and still work with high efficiency (up to 99.5%) [34]. The LFT main function consists in regulating the voltage to the desired level through a tap changer. For instance, the voltage must be increased at the generation stage so the power can be fed into a High-Voltage (HV) transmission line. This lines may be up to hundreds of kilometres in length, which would translate to an extremely significant energy loss were they not working at HV. The LFT is also implemented at the distribution stage, usually in substations near the power demand. The HV is then stepped down to the desired level to be fed to distribution lines, which supply industrial, commercial and residential users.

Although the electrical power system has been highly reliable, it is undergoing a transition. As society struggles with ever-increasing challenges due to global warming, environmental agreements, such as the Kyoto and Paris Agreements, were implemented in several world nations. Thus, governments are pushing for Renewable Energy Sources (RES) (*e.g.*, photovoltaics, wind turbines, etc.) to be incorporated in our traditional fossil fuel-based power system. Moreover, the decentralization of power generation, known as *microgeneration*, incentivizes the creation of new enterprises within the energy sector. In Europe, this was mainly possible through the market liberalization [34].

Nonetheless, these developments cause the network layout and operation to become more complex. According to the International Renewable Energy Agency (IRENA), such a transition should address four major challenges [1]:

- Enabling bidirectional energy flow;
- Improving grid interconnection - namely, integration of Distributed Energy Sources (DES)

and communication systems within the network (Smart Grids);

- Adopting enhanced technologies - mainly those of considerable electrical loads, for instance, the electric vehicle in the transport sector or the heat pump in the heating sector [23];
- Increasing Energy Storage Systems (ESS) - crucial for peak demand response in a decentralized scenario.

Moreover, DES integration also results in Power Quality (PQ) issues, particularly, power flow control or the injection of overvoltages to the end-user. The latter usually occurs during off-peak regimes and may be mitigated through a decrease in the output energy or, in extreme cases, by disconnecting them from the grid. However, these solutions translate into less rentability for the exploring enterprises, since they extend the return on investment, disincentivizing the exploration of RES [27]. To simultaneously address IRENA's four challenges and solve DES integration issues in future smart grids, the LFT must be replaced by the Solid-State Transformer (SST).

The main discrepancy in these two technologies comes down to their volumes. The LFT is known for its bulky size, limiting its implementation in certain critical size applications. The SST is equipped with a High-Frequency Transformer (HFT), which allows for a quicker and more dynamical voltage control while also providing galvanic isolation. This contrasts with LFTs, which depend on mechanical tap changers and have limited voltage control (*e.g.*, switching between applications with considerable differences in voltage needs would require a completely new tap changer). Moreover, the High-Frequency (HF) is responsible for the SST's major size reduction, up to 80% [18]. Naturally, its reduced size translates into higher portability, lower installation costs, and easiness in the assembly process, specifically in certain areas such as in offshore applications [18]. Although the first generation of SSTs comes at a higher cost, the decreasing price in semiconductors and control circuitry will gradually allow for SSTs' overall price decrease [34]. Arguably, the SST structure has a higher degree of complexity due to the high number of switching devices, resulting in less reliability and efficiency (up to 98% [34]. Nevertheless, the LFT does not provide a large part of the ancillary services[1] and features that the SST does, which vastly increase the PQ and are crucial for the transition mentioned above.

Some of the SSTs' characteristics absent in LFTs include disturbances blocking, such as harmonics or voltage sag, and power flow control, either active or reactive. Reactive power control allows the regulation of the power factor, independently of load characteristics. Additionally, SSTs may be equipped with a Direct Current (DC) Link allowing for DC applications' integration, such as RES, ESS, or, more recently, DC transmission lines. For such purposes, the LFT would first have to be connected to additional converters, resulting in larger sizes, higher costs and lower efficiency and reliability.

The sections that follow provide an overview of the state of the art in SSTs. Various topologies of this developing technology will be demonstrated, along with its auxiliary services (*e.g.*, power

[1] Ancillary services - necessary services to support electric power transmission from generators to consumers, considering the control area obligations (*e.g.*, line frequency) and transmitting infrastructure requirements. These are key to maintain the system's operation reliability [30]

output control, voltage regulation). The fundamental component of the SST, the HFT, is also discussed, as well as the major design issues it faces. The dissertation objectives are presented after an examination of current SST applications.

1.2 State of the Art

1.2.1 Solid-State Transformer

The concept of a ”solid-state transformer” was first discussed in 1968 by W. McMurray, when he introduced a device based on solid-state switches. He introduced an Alternating Current (AC) converter with HF isolation that behaved like a traditional transformer [31]. The first real application for the SST appeared later, in the 1990s, in traction systems, where the traditional LFTs provided a bulky, heavy, and space inefficient solution. Engineers found solutions for these issues in the development of SST applications [23].

Considering the development of power electronic circuits and devices (*e.g.*, Silicon Carbide (SiC) MOSFETs), the SST becomes a viable option to replace the LFT in the power distribution system. Moreover, they bring several other ancillary services which provide the system with better PQ.

Depending on the application, a SST has different configurations, having several power conversion steps. Most topologies use an HFT that provides galvanic isolation to the system and is responsible for most of the size reduction compared to an LFT [29] [27]. The SST base functioning consists of converting a low-frequency voltage input, usually grid supplied (50-60 Hz), into a HF voltage. This process happens through switching circuits equipped with semiconductor devices. Alternatively, the voltage may also be first rectified and supplied to a HVDC-link and be later converted into HF. This HF alternating voltage is then applied to the HFT’s primary side so the system can bring the voltage to the desired level. The induced voltage on the HFT’s secondary side is then rectified to supply a DC-link. At this point, the DC-link power can either supply DC loads or integrate DC-DES (*e.g.*, photovoltaics) or connect with an AC-link through another converter for load or generation purposes. For DES integration bidirectional power flow must be enabled. A basic structure of the SST is represented in Fig.1.1.

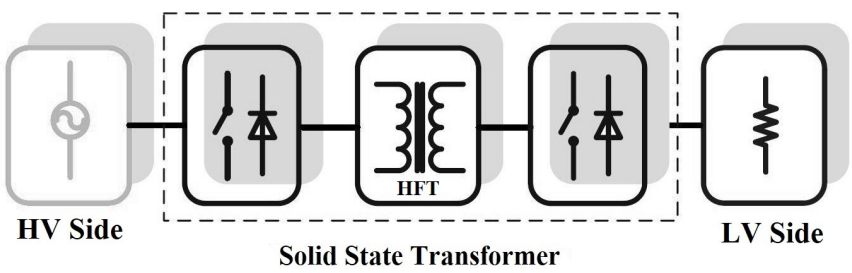


Figure 1.1: Basic Structure of the SST based on [36].

Considering possible applications on which the SST can link DC and AC systems running at medium and low voltage levels, several combinations are possible. For instance, the device can be

used to link Medium-Voltage (MV) and MV, MV and Low-Voltage (LV), or LV and LV, DC and/or AC systems. It is noteworthy that AC systems can be multi-phase, which increases the complexity of the design [13].

1.2.2 Overview of SST architectures

Selecting the appropriate topology is crucial when it comes to SST implementation. To tackle this issue, engineers should consider the application's needs to minimize cost, maximize efficiency, and make the system more flexible to future changes. Such topologies can be classified according to the number of conversion stages to be installed: Single-stage, Two-stage with LVDC or MVDC-link, and Three-stage. Their basic scheme is represented in Fig.1.2.

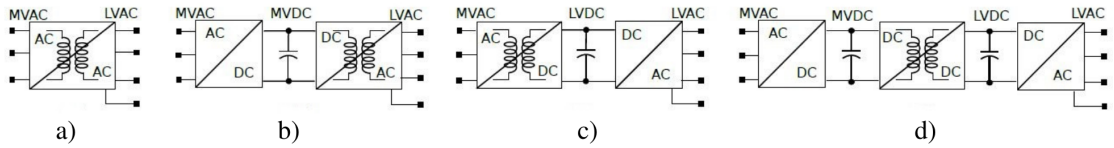


Figure 1.2: SST configurations: a) Single-stage, b) Two-stage with MVDC-link, c) Two-stage with LVDC-link, d) Three-stage. Image taken from [33]

.

If HV functioning is considered (*e.g.*, power distribution), the device switches would not be compatible due to the high blocking voltage applied, exceeding their nominal rating. Also, high power applications test the boundaries of the components. The solution consists of a modular multilevel configuration to share the electrical quantities between the modules. These can either be based on Input Series Output Parallel (ISOP), Input Parallel Output Parallel (IPOP), or Input Series Output Series (ISOS). These are illustrated in Fig.1.3. Regarding the conversion stages, it is worth noting that these SST configurations still fall into the four categories mentioned above.

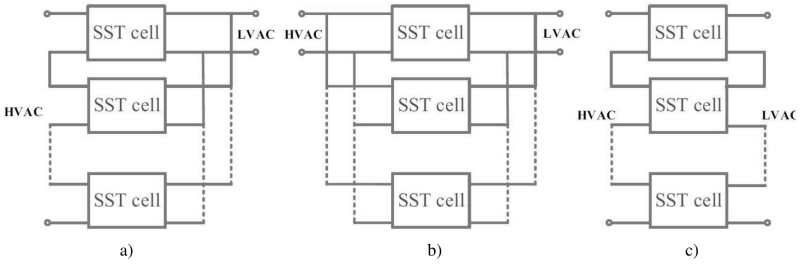


Figure 1.3: SST modular-multilevel configurations in HV and high-power systems: a) ISOP, b) ISOS, c) ISOS. Image taken from [36].

Each topology will be briefly reviewed in the following sections, including their base configurations, applications, advantages and disadvantages.

1.2.3 Single-Stage Topology

Single-stage is the simplest SST topology. It comprises one power conversion through an HFT, which connects the MV to LV, allowing for bidirectional power flow and providing galvanic

isolation to the system. The single conversion device can operate in direct DC-DC or AC-AC conversion. A basic schematic of this topology is represented in Fig.1.2 a).

Due to fewer switching devices, which result in lower conduction and switching losses and a considerably cheaper cost [26], this topology has higher efficiency and reliability than the Three-stage topology [18]. The control system uses the shift angle to control the direction and magnitude of the power flow. Moreover, in bidirectional power flow, four-quadrant switches are necessary, which improve control strategy and Total Harmonic Distortion (THD) [18].

Regarding AC-AC converters, such as the full-bridge converter, these are characterized by high switching frequency which allows for a smaller sized HFTs. Additionally, there is no need for an electrolyte capacitor, making this setup more suitable for critical size applications. Soft switching is also achieved only for limited bandwidth around the rated load, making this application more suitable for constant load situations [2].

Due to the lack of a DC-link, AC-AC converters are unable to connect with the DC grid, DC transmission and DC local storage. As a result, the integration of RES is limited in this topology. Furthermore, without a DC bus, some auxiliary services like as reactive power regulation and disturbance blocking (*e.g.*, voltage sag and harmonics) are lost. [26][14].

Furthermore, the majority of SSTs are built for MV operation (*e.g.*, 7.2 kV AC). In a Single-stage structure, however, this causes voltage stress on switches. This requires modular multilevel designs, such as the ones described in the previous subsection, in which the voltage and power are shared in series. Nonetheless, because power and voltage must be balanced throughout the setup, this solution demands complex control. Two-stage and Three-stage topologies are required to overcome such problems [18].

1.2.4 Two-Stage Topology

A DC-link is introduced on either the MV or LV side of the Two-stage topology, which distinguishes it from the Single-stage architecture. Although this setup allows for bidirectional power flow, it may simply be switched to unidirectional by using an unregulated rectifier on the AC-DC converter's LV side [18]. A fairly complex switching approach and a large number of switching devices usually come with a double staged topology. Nonetheless, such complexity results in additional useful auxiliary services like reactive power compensation [14].

1.2.4.1 Two-Stage Topology with LVDC-link

As its name suggests, the Two-stage topology with an LVDC-link comprises of two conversion stages. First, the supply AC voltage is converted to a higher frequency so that the HFT can regulate the power to the desired voltage. Then, the output voltage from the LVAC side of the HFT gets rectified and supplies the LVDC bus. This constitutes the first conversion stage. In the second stage, the DC voltage in the DC-Link is inverted by the DC-AC converter [14]. A basic schematic of this topology is represented in Fig.1.2 c).

This architecture provides reactive power compensation, good output voltage and input-current regulation [14]. Moreover, due to the presence of a DC-Link at the LV side, this topology allows for the interaction with DES, RES (*e.g.*, photovoltaic and wind plants), ESS and DC loads capable of bidirectional power flow [14] [18].

Like the Single-stage topology, this Two-stage architecture is not suitable for HV operation, considering that it is hard to achieve the necessary Zero Voltage Switching (ZVS) in the inversion process in such an extensive input range. Furthermore, well-established multilevel topologies cannot be easily applied to the HV side. Thus, high switching losses may not be avoided without sacrificing frequency, leading to lower efficiency and difficult thermal management [36]. However, removing the LVDC-link is counter-productive as it would translate into poor RES integration, as discussed in the Single-stage section. The HVDC from end-applications may present HV issues. These can be addressed by converting the current to LVDC, instead of LVAC, and connecting it directly to the DC-link [18]. Furthermore, high complex control systems are necessary to control the bidirectional flow, and a high ripple current in the DC-link is usually present [14].

1.2.4.2 Two-Stage Topology with MVDC-link

This topology shares most of the previously mentioned architecture benefits, as it also contains a Two-stage conversion system and a DC-Link. However, the DC-Link is now on the MV side. Thus, galvanic isolation and voltage step-down are preformed at the DC-AC conversion stage. Therefore, the LVDC link is no longer available [36]. A basic schematic of this topology is represented in Fig.1.2 b). Such configuration is not so suitable for integration of the DES, RES and ESS. Instead, thanks to the MVDC link, it is suitable for applications in the distribution grid, such as in the integration of MVDC grid transmission lines [14].

1.2.5 Three-Stage Topology

Due to its several ancillary services and features, this topology is the most popular amongst SST architectures. Not only does it have a significantly lower weight and size than the traditional LFT, but it can also optimize its performance in distribution and transmission grids [18]. In similarity to the two topologies previously mentioned, the Three-stage design also allows for bidirectional power flow. This architecture incorporates an AC-DC conversion stage, a DC-DC conversion stage with an HFT, which provides galvanic isolation, and a DC-AC conversion stage [26].

Two DC links are connected to each side of the DC-DC conversion stage. These decouple the MV side from the LV side, avoiding propagating disturbances from the grid to the end-application or vice versa. A basic schematic of this topology is represented in Fig.1.2 d). Moreover, this design can address power PQ issues, such as reactive power compensation and voltage sag compensation. It also allows for voltage regulation, current limiting, and load protection. The DC-Link in the MV side makes the application suitable for integration in distribution and transmission grids. On the other hand, the DC-Link in the LV side allows for integrating DES, RES and ESS applications.

Thus, this topology is considered the most versatile [36] [14] [18]. However, due to the higher number of switching devices, it has a higher cost and lower efficiency [18].

1.2.6 SST Topology Comparison

Given the three architectures' essential descriptions, they may be compared by evaluating the available functionalities, limitations, and feasible applications of each one.

The Single-Stage topology allows bidirectional power flow, but its application on RES and DES is minimal due to the lack of a DC-link. This also translates into a lack of functionalities, such as reactive power compensation. Nevertheless, its low number of switching devices allows for size reduction and provides high efficiency and reliability.

The Two-Stage topology describes an intermediate topology between the Single-Stage and the Three-Stage ones. The additional DC-link placed at MV or LV allows for many functionalities, such as the reactive power compensation, limitation of disturbances propagation, etc. The control scheme becomes more complex than in Single-stage SST since the stages operate at different frequencies.

Lastly, Three-Stage topology is the most versatile in terms of applicability and functionality. However, the higher number of switching devices directly translates into lower efficiency due to switching losses and lower system reliability. Despite its higher cost, this topology has broader applicability, making it most suitable for DES and RES integration. Table 1.1 presents a summary of the three architectures' functionalities and applications.

Table 1.1: SSTs' topologies capabilities comparison [18] [23] [14] [34].

Capability	Single-Stage	Two-Stage	Three-Stage
Bidirectional power flow	Yes	Yes	Yes
Reactive power compensation	No	Yes	Yes
Independent power factor	No	Yes	Yes
Independent frequency	No	Yes	Yes
Input current limiting	No	Yes	Yes
Output current limiting	No	Yes	Yes
Input current regulation	No	Good	Very Good
Output voltage regulation	Poor	Good	Good
Harmonic and voltage sag limitation	No	Good	Very Good
Modularity implementation	Simple	Hard	Simple
DES applications (such as RES)	Not suitable	Suitable	Suitable
Grid applications	Suitable	Suitable	Suitable

1.2.7 Overview of the Connection Stages

1.2.7.1 MVAC - MVDC connection stage

This stage connects the MVAC side (usually grid line, 50/60 Hz) with the MVDC link through the active rectifying process, which allows for bidirectional power flow. Also known as the medium voltage stage, this stage enables the SST to filter out reactive power in the MV grid, using only active power and feeding it on to the next stage.

Multilevel converters stand out as a solution for this phase due to their high power ratings, lower Common-Mode Voltage (CMV), reduced harmonic content, near sinusoidal currents, small input and output filters (if necessary), increased efficiency and possible fault operation [31]. Regarding existing multilevel converter topologies, Table 1.2 provides a comparative overview of the most relevant for SST applications. Furthermore, their circuit schematics are presented in Fig.1.4.

Table 1.2: Comparison between the different AC-DC converters [18] [14] [23] [31].

AC-DC Converter	Advantages	Disadvantages	Application
Neutral-Point Clamped (NPC)	- Simple control; - Presence of a DC-link; - High power density; - Lower cost.	- Larger AC filter; - Lower PQ; - Higher switching voltage; - Energy inefficiency; - Voltage unbalance issues for more than 3 levels.	Medium Voltage
Cascaded Half-Bridge (CHB)	- Simple control; - Low-frequency operation for each cell; - Good control functionality at medium cost.	- Need for isolated supply for each cell; - Absence of a DC-link.	Medium Voltage
Modular Multilevel Converter (MMC)	- Lower frequency operation; - Presence of a DC-link.	- Complex control; - Bulky Capacitors; - High cost due to more devices and capacitors.	High Voltage

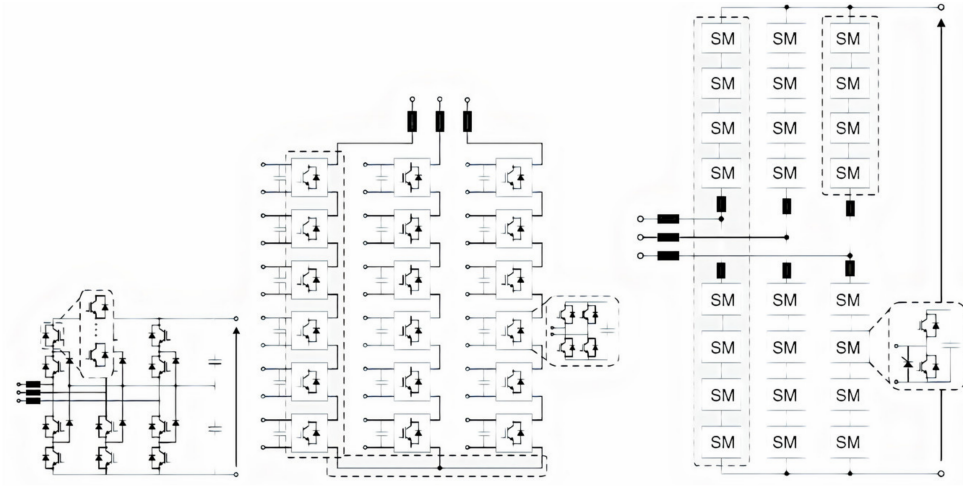


Figure 1.4: Circuit schemactic of AC-DC converters: a) NPC; b) CHB; c) MMC. Taken from [23].

1.2.7.2 MVDC-LVDC connection stage

This stage is at the core of the SST design. It is composed of a high-frequency converter which serves as the power flow control between the MV and LV grids. The HFT is also part of this stage, bringing the converter's input voltage to the desired level through HF AC power [18] [14] [23]. This conversion stage is composed of there parts: a DC-AC converter, an HFT, and AC-DC converter;

This conversion stage is also the most challenging for SST design since the application's high-power requirements translate into high-current on the LV side and HV on the MV side. Two approaches to meet these high-power requirements have been investigated. The most straightforward solution is to use standard HV-rating devices. However, one can opt for a modular concept. This solution consists of cascading several LV device modules to share the total voltage and power. Additionally, it presents a high number of switching devices resulting in lower reliability. However, it also has several advantages: low electromagnetic interference, streamlined fault tolerance strategy and the usage of standardized LV rating devices, which are easily available and simplify modular implementation [23] [18]. Regarding existing topologies, Table 1.3 provides a comparative overview of the most relevant for SST applications. Furthermore, their circuit schematics are presented in Fig.1.5.

Table 1.3: Comparison between the different DC-DC converters [18] [31] [23] [26] [38].

DC-DC Converter	Advantages	Disadvantages	Efficiency
Dual-Active Bridge (DAB)	- Simple control; - Controllable power flow; - Less reactive power flow.	- Less efficient due to higher number of switches; - Higher leakage inductance; - Less transformer saturation.	92.5%
DAB with Series Ressonant Converter (SRC)	- Well regulated output voltage; for a wide range of loads; - Reliable; - Higher switching frequency; - No issues in inductance leakage; - Protected against transformer over-saturation.	- Incapable of regulating output power; - Complex control; - High resonant capacitor.	98.61 %
Dual-Half Bridge (DHB)	- Less number of switching devices; - Higher reliability ; - Lower cost.	- More reactive power; - Blocking voltage limitation; - High current through transformer windings.	96%
Asynchronous Quadruple -Active Bridge (AQAB)	- Less number of switching devices; - Higher reliability; - Controllable power flow.	- High-power rating devices are necessary.	97.5%

Some other topologies also are worth mentioning, such as the three-phase DAB and the multiple-active-bridge (MAB) converter. The three-phase topology may be adopted due to lower device stress, more efficient transformer usage and lower filter requirements [26]. The MAB converter has the same features as the three-phase DAB converter, but it reduces the number of HF transformers by linking more active bridges into a single transformer [23].

The modularity flexibility at this stage is key for the application's versatility. Multiple DC-

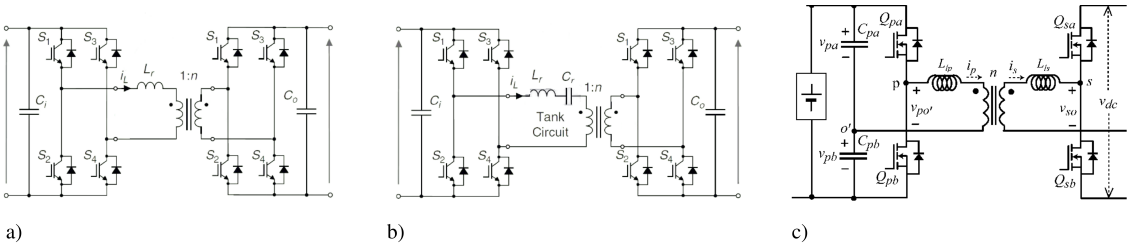


Figure 1.5: Circuit schemactic of DC-DC converters: a) Dual-Active Bridge (DAB) [23]; b) DAB with SRC [23]; c) DHB [21].

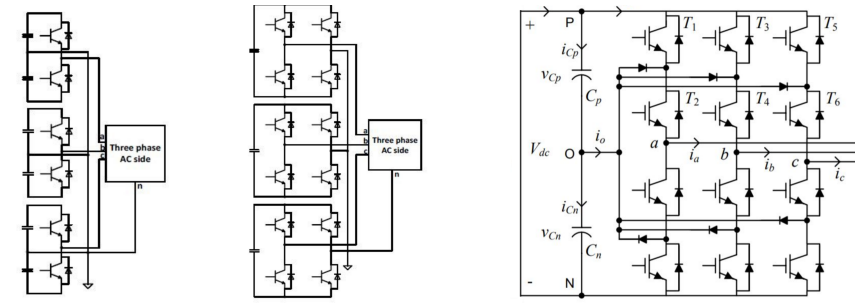
DC converters can be used to create more complex structures, as the application's necessities vary. Moreover, a parallel connection can be used on the MV side and a series connection in the LV side to reduce the LV side's voltage ripple. This is mandatory for single-input and single-output topologies such as the DAB, DHB and SRC-DAB converters. MAB converters introduce a higher degree of flexibility [23].

1.2.7.3 LVDC-LVAC connection stage

It is responsible for converting DC to AC. The power can be transferred from or to the DC-DC stage converter. The output terminal from the DC stage is often connected to AC loads, but it can also integrate DES. The voltage level can vary according to the application. Multilevel topologies can be adopted depending on the application. If HV is involved, modules should be cascaded to share the total voltage so the switching devices can withstand the HV rating. If the applications integrate AC loads, four-leg (three-phase plus the neutral conductor) topologies should be adopted. This stage plays an essential role in the SST's application as it is responsible for shaping the DC voltage into a sinusoidal AC waveform with the desired amplitude and frequency. The inversion process is not affected by any possible disturbances (*e.g.*, overvoltage or voltage sag) and other systems connected to the supply grid [18], since the HFT provides galvanic isolation. Moreover, if the AC output waveform needs to be improved more modules can be installed. The modularity approach is always an advantage as it presents a flexible solution for future variations in the application's power. Regarding existing topologies, Table 1.4 provides a comparative overview of the most relevant ones for SST applications. Furthermore, their circuit schematics are presented in Fig.1.6.

Table 1.4: Comparison between the different DC-AC converters[18] [31] [23] [26] [37] [14].

DC-AC Converter	Advantages	Disadvantages
Half-Bridge (HB)	- Most simple of all topologies; - Less number of switches; - Higher Reliability.	Voltage unbalance issues.
Full-Bridge (H-bridge)	- Lower DC-link voltage.	Voltage unbalance issues.
Neutral-Point Clamped (NPC)	- Enables the use of 600V power devices; - Increased system's efficiency; - Reduced voltage sag and THD.	Neutral-point voltage unbalancing.



a) b) c)

Figure 1.6: Circuit schemactic of DC-AC converters: a) HB [31]; b) H-Bridge [31]; c) NPC [19].

Three-level topologies are the most feasible options with regards to applicability [23]. Thus, the HB and H-Bridge inverters may be connected in parallel to form multi-phase converters, including three-phase systems as represented in Fig.1.6. However, in some architectures, such as the HB and FB , this implies more DC-links, which directly influences the remaining stages in the application.

1.2.8 High-frequency transformer

The HFT is at the core of the SST, replacing the traditional 50/60 Hz transformer and decreasing overall weight and volume. Moreover, it provides galvanic isolation to the SST's end application. The principle behind the functioning of the HFT is the same as in the traditional transformer, as expressed by Faraday's induction law 1.1. However, as the magnetic field's frequency crossing the transformer's windings is much higher than in a traditional LFT, the number of necessary windings to achieve the same voltage level transformation is much lower [18]. The basic HFT operation is shown in Fig.1.1.

$$\varepsilon = -N \cdot \frac{\Delta\phi}{\Delta t} \tag{1.1}$$

The higher-frequency operation makes the design of the HFT much more complex than the traditional LFT. Several design measures should be taken into account for this HV, high-power, and HF functioning.

During the HFT manufacturing process, **material selection for the core** is based on loss reduction (Foucault currents and Hysteresis phenomenon), saturated magnetic flux maximization (usually translating to higher power density), Curie and maximum operating temperatures, and magnetic permeability maximization [14] [18] [27]. Nanocrystalline proves to be the best material choice due to its high saturation flux density and lowest power losses. [18]. However, its high cost and limited design customization should be considered [36].

Winding configuration should also be carefully studied. Mutual inductances and windings' coupling coefficients are directly influenced by winding placement, affecting power loss and system efficiency. A popular SST application is core-type solenoidal structures for their low cost, and

easy manufacturing process [18].

Wire material selection is also a crucial consideration. Two key challenges arise due to HF functioning: the skin effect and the proximity effect [12]. Such effects can not be ignored, as they largely affect the system's performance. A Litz wire is implemented to suppress them, as it contains hundreds of smaller and properly isolated conductive strands (down to 0.005 mm^2 cross-section area) [18]. Taking voltage power calculations into account, the strands can be agglomerated into a thicker wire with the desired overall cross-section. Each strand's cross-section is quite small compared to penetration depth, making the AC flow roughly homogeneous across them and thus, the total cross-section, directly suppressing the skin effect. Moreover, to minimize the proximity effect, the wire is then twisted and woven [14].

Although the above-mentioned methods aim to minimize parasitic phenomena, some cannot be ignored when mathematically modeling the HFT. For a core-type HFT with unity-turns ratio, a model was developed considering the parasitic quantities, presented in Fig.1.7.

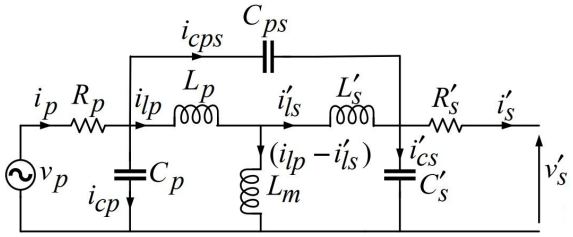


Figure 1.7: HFT equivalent circuit schematic referred to primary. Taken from [22]

.

Regarding the circuit, v_p represents the primary excitation voltage, and v'_s the secondary voltage. L_p, L'_s and L_m represent the primary and secondary windings, respectively, and mutual leakage inductances. These represent the imperfect magnetic linking between windings. C_p and C'_s represent the stray capacitances across each winding. Cps represents the stray capacitance between windings. All three capacitances arise from the electric potential differences between nearby surfaces, close enough to generate an electric field.

Moreover, other design elements can be considered for space-limited applications, such as **HV isolation between primary and secondary windings and thermal management**. Regarding isolation, a dry-type transformer design is only suitable to a certain extent. If necessary, insulating materials should be considered, such as epoxy or highly insulating wire [36]. In such applications, oil-free functioning is expected. Consequently, thermal management becomes a challenge in the SST design. If feasible, natural convection is the simpler and preferred solution. However, other more powerful approaches may be necessary, such as fan-cooled and water-cooled heat sinks [36].

1.2.9 SST Applications

Regarding functionality, the SST is well suited to replace the traditional LFT and other power electronic converters within the distribution system, allowing for a more compact and integrated

system. The SST's efficiency and cost discrepancy is justified by its several additional features and ancillary services. This increased versatility translates into broader applicability. Most of new SST applications exploit its advantages regarding better controllability, smaller necessary working space and integration capability in both AC and DC systems. The main SST applications are summarised in the following categories:

- **Smart Grid:** As mentioned in the introduction section, RES gain increased interest in the context of environmental concerns and the search for a more sustainable electrical power system. As some of the RESs are generated in DC power (*e.g.*, solar photovoltaic panels), bulky converters and inverters would be necessary to achieve grid connection if a traditional LFT was used. The SST is a viable solution to this inconvinience, as it allows for DC integration and for the necessary power conversions. More importantly, it is worth noting that RES are not continuously generating energy. Moreover, conventional RES systems would disconnect during overvoltages periods, decreasing profitability for exploring enterprises. Once more, the SST offers a solution to this challenge, as it can control the output power and provide disturbance shielding [18]. The SST has also shown to be suited in wind-powered generation systems, since these systems usually require extra circuitry for reactive power compensation, besides the already necessary voltage transformation devices for grid connection. Therefore, the STT provides a variety of smarter, more efficient and more compact solutions to a range of challenges present in LFT applications [36]. Moreover, the SST's LVDC-link could allow the integration of other types of DES and ESS.

- **Power Quality**: As presented in earlier sections, the SST may provide reactive power compensation depending on the adopted topology. Furthermore, it can also provide harmonic current filtering depending on the adopted switching frequency. Finally, the SST enables fault isolation and limitation if equiped with the respective control functions, as opposed to the passive LFT.

- **Traction System**: Traction systems are indeed one of the major SST's applications. The current systems use bulky LFTs, for instance, a 6 MVA LFT has a weight to power ratio of 1.7 kg/kVA (depending on the frequency), making its average weight around 10 Tones [18]. Thus, in such critical-sized applications, researchers are pushing for SST systems, providing size and weight reduction without compromising efficiency.

1.3 Dissertation Objectives and Structure

The goal of this dissertation is to develop, design, and simulate a Two-stage SST for connecting a battery storage system to the AC grid. The system must provide bidirectional power flow as well as meet minimal PQ standards (*e.g.*, input current harmonic distortion, voltage stability).

The introduction chapter starts by exposing the context & motivation behind the study of SST technologies which will be a crucial part of the electrical sector as it transits to a more sustainable and green reality. Following that, a brief state-of-the-art of SST technology is offered including its

various topologies based on the number of conversion steps used. There is also a breakdown of the connecting stages and the many sorts of converters utilized in each. The HFT, which is at the heart of the SST, is also briefly discussed, as are its primary design and modelling features. Finally, the most trending SST applications are discussed.

In chapter 2, the system is explained in detail. The configurations of the converters employed in each connection stage are discussed, as well as their primary design challenges and requirements.

In chapter 3, the modelling of the system is developed. A mathematical model is presented for the various converters employed in each stage.

In chapter 4, the control techniques employed in each converter are described in full detail.

In chapter 5, a simulation of the proposed system is presented, followed by a discussion of its respective results.

Finally, in chapter 6, a perspective on the already accomplished work is provided, as well as a proposal for future work.

Chapter 2

Proposed System

To integrate a Battery Storage System (BSS) into the HVAC electrical grid, the proposed system is a two-stage conversion SST. To further understand the system, a simplified block diagram is shown in Fig.2.1.

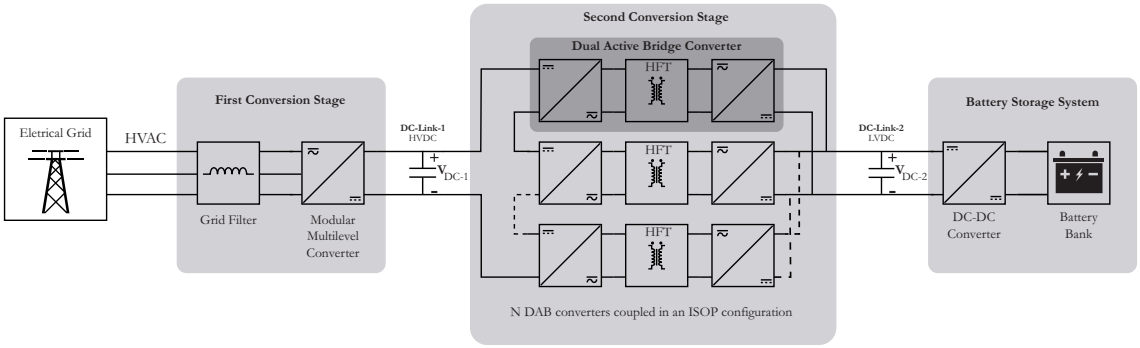


Figure 2.1: Proposed system to integrate the BSS to the HVAC electrical grid.

Due to the lack of a neutral connection in HV systems, the initial conversion step connects a three-phase system made up of three wires. The initial stage of conversion must meet minimal PQ standards, satisfy grid requirements and allow bidirectional power flow. When the BSS is in charging mode, electricity is rectified from the AC grid to the DC-Link-1 (HVDC), and when the BSS is delivering power, power is inverted from the DC-Link-1 to the HVAC grid.

The second conversion stage connects the DC-Link-1 (HVDC) to the DC-Link-2 (LVDC). As a result, it is made up of N_{DAB} converters connected in an ISOP, thus the converters share the DC-Link-1 voltage in series, and the DC-Link-2 current in parallel. To provide bidirectionality, converters must be able to manage power flow from or to each DC-Link. Each converter requires an HFT with a transformation ratio near to unity to provide galvanic isolation between the electrical grid and the BBS.

The BSS has a lower operating voltage and several operation modes, which means it can work with varying working voltages and currents. As a result, in order to discharge and charge the

battery pack properly, the BSS requires the inclusion of a DC-DC converter.

The sections that follow provide justifications for the topologies employed in each stage, as well as a brief overview of their underlying configuration.

2.1 First Conversion Stage

The Modular Multilevel Converter (MMC) is an attractive topology for several applications in the energy field. The converter's base architecture characteristic is a cascade connection of Submodule (SM), which gives it modularity, scalability, and flexibility. Such features were critical in selecting this type of converter for the first conversion stage, since the modular topology allows the converter to operate over a wide voltage and power range, making it appropriate for the HVAC-HVDC conversion stage [11].

The converter does not require separate DC sources, hence no special transformer is required. Since each module has its own capacitor, the modular architecture reduces the requirement for HV capacitors, greatly reducing the cost of the application. Regarding PQ, the converter is able to generate line-to-line voltages and grid currents with low harmonic content. Depending on the chosen control strategy, it may offer low filter requirements in function of the converter's switching frequency [4].

The number of SMs in an MMC varies depending on the application, operating voltage and semiconductor device rating. 5 SMs/arm are required for a 3.3 kV operational voltage motor drive. HVDC applications, on the other hand, can require up to 400 SMs/arm to handle voltages up to 400 kV. The MMC can produce a DC-Link-1 voltage waveform with a very high number of voltage levels as the number of SMs rises. As a result, the SMs can be operated at a lower frequency reducing the converter's losses. Furthermore, depending on the number of SMs employed, it can use redundant SM in each arm to ensure fault tolerance [6].

The next section makes a brief review of the MMC's configuration along with its functionality.

2.1.1 MMC Configuration

The MMC is a three-phase AC-DC converter and its configuration is represented in Fig.2.2. It consists of three legs, and each leg is divided into two arms: upper (u) and lower (l). Each arm is comprised of a series connection of SMs with an inductor (L_m). This component, "L_m", can also be referred to as an arm inductor, and its power losses are represented with a resistance of "r_m". This inductor is placed mainly to limit the magnitude of Circulating Current (CC) flowing through the arms due to the instantaneous voltage difference between the arms [11].

All converters legs have their positive and negative bus terminals connected to a common DC system. Such a system is represented by an ideal split DC source of voltage rated $\frac{V_{DC-1}}{2}$. The DC cable is represented with an inductor "L_d" and an equivalent resistance "R_d". The midpoint of each converter leg is an AC output terminal (a, b, c). Each terminal is connected to a grid filter,

represented by "L_f" and "R_f", its necessity and functionality are discussed in subsection 2.1.3. The filter then connects to the grid, represented by an AC voltage source rated V_g in all three phases. The grid source is configured in the star connection, and their common point is referred to as "n". However, since the converter is connected to HVAC grid, this point is inaccessible and is merely representative for the discrete-time modelling of the converter, which is explored in detail in chapter 3.

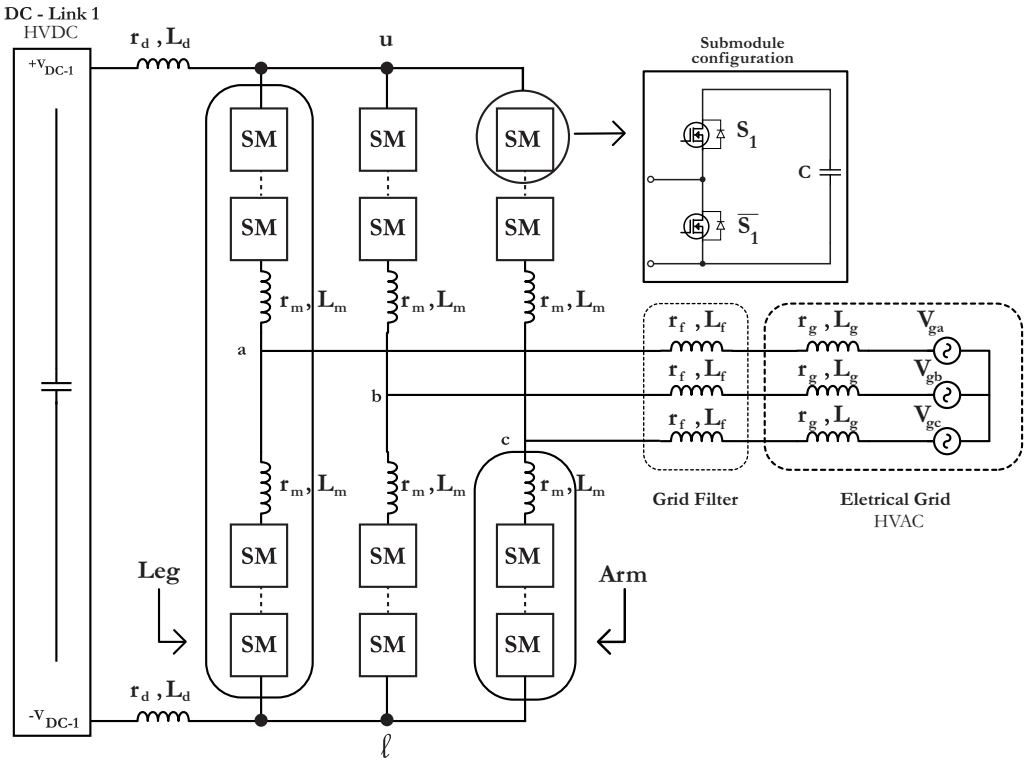


Figure 2.2: MMC & SM configuration.

2.1.2 Configuration of SMs

Over the last few years, various SM configurations have been produced. However, due to its low number of components, easy control and high efficiency, the Half-Bridge Submodule (HB-SM) has proven extremely popular in various applications [6]. The HB-SM, also known as chopper cell, consists of two MOSFETS (S_1 and $\overline{S_1}$) with an anti-parallel diode and a floating capacitor (C), as shown in Fig.2.2. The two MOSFETS are operated in a complementary manner, thus an independent gating signal is sufficient to control the HB-SM. The discrete-time modelling of the HB-SM is also necessary for the chosen control strategy and is explored in subsection 3.1.2.

2.1.3 Grid Filter

To connect to the HVAC grid, the SST application requires a filter. This filter primarily serves three purposes. The first is to allow active and reactive power control between the SST. The second function is to diminish the SST's harmonic distortion in order to maintain PQ, as the converter's line-to-line voltages are not sinusoidal like the AC grid voltages [4]. The filter's final duty is to

serve as a charging element, allowing the converter to convert HVAC power to HVDC since the HVDC-link rated voltage is higher than the HVAC peak voltage.

The L-filter, LC-filter, and LCL-filter are the three basic filters that can be used to connect the SST to the electrical grid [3]. Taking into consideration the MMC's architecture, the switching frequency increases as the number of SMs grows, allowing for more sinusoidal waveforms. As a result of these two qualities, harmonic distortion is minimized and filters are smaller. The high switching frequency guarantees proper filtering and allows for compact filters, resulting in a minimal voltage drop across the filter inductor [4]. Consequently, a simple L-filter can be used to link the converter to the HVAC grid, ensuring attenuation of -20dB/decade across the whole frequency range [3]. Furthermore, because HV capacitors are expensive, a filter with a capacitor should be avoided whenever possible to reduce costs.

2.2 Second Conversion Stage

Because the proposed system is a HV application, the stage connecting the battery pack to the HVDC-link must comprise a set of DC-DC converters capable of bidirectional power flow, coupled in an ISOP philosophy, as previously described. Since the converters are connected in series, the HV from the DC-Link-1 can be shared between the converters, and the resultant larger currents on the DC-Link-2 side can be shared via a parallel connection.

Different topologies exist for DC-DC converters; nevertheless, galvanic isolation is a condition that excludes all non-isolated topologies. Furthermore, resonant topologies were omitted since they require an additional capacitor, resulting in a bigger, heavier, and more expensive solution [15]. As a result, the DAB converter and its half-bridge variant are the only options. Even while the latter option uses fewer switches, it necessitates the use of split capacitors, which inevitably increases the size and cost of the application [5]. The following section will present a brief review of the DAB converter configuration.

2.2.1 Dual-Active Bridge

The DAB is a bidirectional, controllable DC-DC converter with high power capabilities. It comprises eight semiconductor devices, an HFT, an energy transfer inductor, L_{DAB}, and DC-link capacitors. This converter can be more commonly described as a full bridge with a controllable rectifier. Due to its symmetry, with identical primary and secondary bridges, it is capable of bidirectional power flow control [16].

The topology is shown in Fig.2.3, with V_1 and V_2 denoting the DC-link voltages, L_k denoting the transformer's leakage inductance plus a required external energy transfer inductor, L_{DAB}, and M_{1-8} denoting the controllable semiconductor switches. IGBTs or MOSFETS could be used in these devices. However, because the latter design incorporates an intrinsic body diode and drain-to-source capacitance, it eliminates the need for additional anti-parallel diodes and snubber capacitors to direct current commutation during switching events and enable ZVS. SiC is a wide

bandgap material with greater voltage, thermal, and turn-on energy ratings, making it ideal for high-frequency switching converter applications [15].

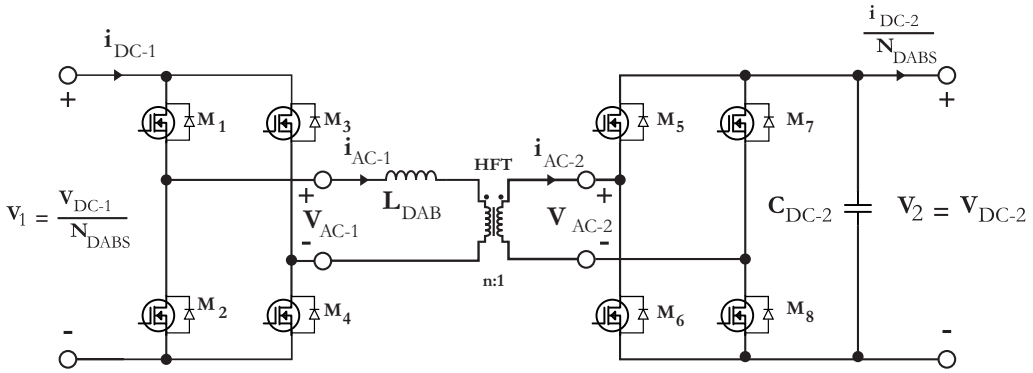


Figure 2.3: Dual active bridge topology.

2.3 Battery Storage System

The BSS is composed of a DC-DC converter and a battery bank of lithium-ion cells as represented in Fig.2.4. A DC-DC converter is required in order to correctly charge and discharge the battery bank. Every type of battery cell has its unique set of instructions for charging and discharging it. With regards of charging, lithium-ion batteries should be charged in a constant current mode until they reach a specified charged voltage. Thereafter, until the battery current reaches the cut-off current, these should be charged in a constant voltage mode [24]. Only the constant current charging regime will be considered since the major focus of this thesis is not to study the charging/discharging regimes of batteries. The bank should be discharged at a constant current until the discharge cut-off voltage is reached for the discharging regime. The bank should then be re-charged. These values differ depending on the type of cell and its manufacturer. However, rate discharge & charge parameters should be respected as they have a significant impact on battery life, safety and functionality [17].

To ensure that the cells are not damaged during charging and discharging cycles, the DC-DC converter should be controlled in relation to the voltage, current and temperature of the battery. For this a simple non-isolated bidirectional buck/boost converter is employed. Composed of only two MOSFETS (T_{1-2}) and a high frequency inductor (L_{BAT}), which filters the battery pack current (I_{BAT}). For this converter ZVS cannot be achieved for both of the switches during continuos conduction mode operation, which leads to high switching loss when operated at HF [32]. This converter is controlled by adjusting the duty-cycle of a Pulse-Width Modulation (PWM) signal, which is applied to the gates of complementary switches T_{1-2}. The charging and discharging regimes must be considered to obtain the duty-cycle of the PWM, this control is further studied in chapter 4.

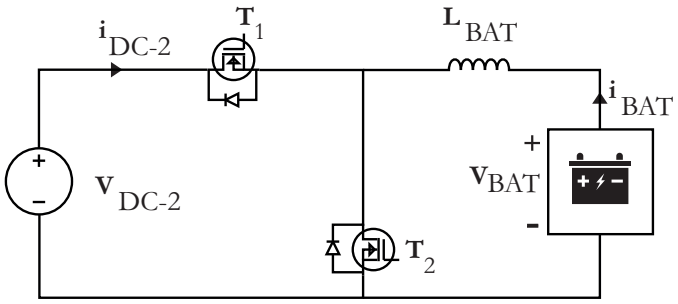


Figure 2.4: BSS configuration.

Chapter 3

System Modelling

3.1 Discrete-time model of the MMC converter

The discrete-time model of MMC is fundamental to implement the chosen control algorithm presented in chapter 4. Depending on the application, operation requirements and available resources, one can choose between two different philosophies to model the converter, the per-phase and the three-phase. The per-phase philosophy is employed in isolated HVDC applications, whereas the three-phase is used in the MMC-base motor drives and grid-connected systems [6]. Because the converter is connected to the electrical grid, a three-phase mathematical modelling is mandatory.

In the studied system, the MMC realizes the connection between the grid (HVAC) and the DC-Link-1 (HVDC). Thus the appropriate philosophy to model the converter is the three-phase. In the three-phase approach, the three-phase equations are solved together to obtain the discrete-time model of the MMC. On the contrary, the per-phase philosophy assumes that the dynamics of current components in each leg are identical. Moreover, per-phase models also neglect the voltage potential between the neutral point of the grid ("n") and the midpoint of the DC-Link-1 ("o"), also known as CMV. Allowing for independent control of each phase, leading to reduced complexity and computational burden [9].

These assumptions hold well under the balanced operation of the system. However, if an unbalance is caused by a variation in load demand or switching action, the DC-Link-1 current will have a ripple, and its distribution is not identical in the three phases . In such scenarios, the DC-Link-1 current control and the AC-CC control should be independent. Since per-phase modelling couples them together, a significant rise of CC and ripple in the DC-Link-1 current and SM capacitor voltage is to be expected during unbalanced operation [10]. Per-phase models do not have enough control variables to mitigate effects from the unbalanced operation.

Furthermore, modelling the CMV term in the AC grid current model is crucial for minimizing the SM capacitor voltage ripple and CC. During the unbalanced operation of an MMC, this term also aids in reducing the DC-Link-1 current ripple [9]. Finally, the three-phase modeling concept

can lower the THD in the converter's line-to-line voltages and grid currents waveforms, as well as improve the converter's dynamic and steady-state performance [6]. The above-mentioned performance benefits further support the decision to model the converter in a three-phase approach.

The following subsections present the three-phase discrete-time model of the converter and its respective SMs & arm voltages.

3.1.1 Modelling of the Converter

As mentioned before, the three-phase equations are solved together to obtain the conveter's discrete-time model. This approach expresses each current component dependence on all the six-arm voltages (V_{xy}) and arm currents (i_{xy}). Thus each arm current consists of DC-Link-1 current (I_{DC-1}), AC-CC (i_{zy}), and AC grid current (i_{gy}) components, where $x \in \{u, l\}$ represents the upper and lower arm respectively, and $y \in \{a, b, c\}$ represents the phase. Analyzing Fig.3.1, the upper and lower arm currents for phase-a are deduced into Eq.3.1 [11].

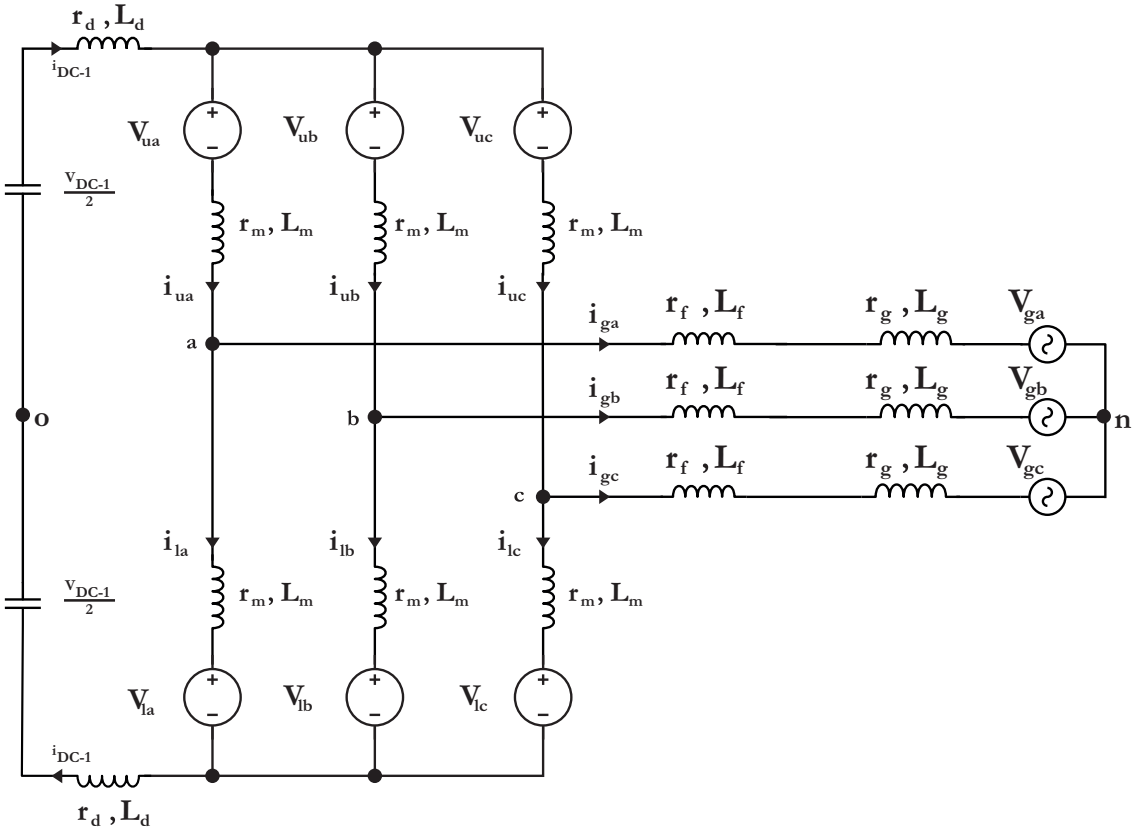


Figure 3.1: Equivalent model of MMC.

$$
\begin{aligned}
i_{ua} &= \frac{1}{3} \cdot i_{DC-1} + i_{za} + \frac{1}{2} \cdot i_{ga}; \\
i_{la} &= \frac{1}{3} \cdot i_{DC-1} + i_{za} - \frac{1}{2} \cdot i_{ga};
\end{aligned}
\tag{3.1}
$$

Contrary to the per-phase philosophy, the three-phase philosophy approach decouples the CC and DC-Link-1 current, allowing for the independent control of both of them. Accordingly, the DC-Link-1 current component is described in terms of the three-phase arm current through Eq.3.2 [11]. In addition, the AC grid currents and AC-CC components based on the three-phase philosophy are depicted in Eq.3.3 [9].

$$i_{DC-1} = \sum_{y=a,b,c} i_{uy} = \sum_{y=a,b,c} i_{ly} = \frac{1}{2} \cdot \sum_{y=a,b,c} (i_{uy} + i_{ly}) \tag{3.2}$$

$$\begin{aligned} i_{ga} &= i_{ua} - i_{la} \\ i_{za} &= \frac{1}{2} \cdot (i_{ua} + i_{la}) - \frac{1}{6} \cdot \sum_{y=a,b,c} (i_{uy} + i_{ly}) \end{aligned} \tag{3.3}$$

In order to obtain the continuous-time model of the MMC converter, the arm voltages should be extracted. In this sense, Kirchhoff's second law is applied to the converter's model represented in Fig.3.1. Taking into account the CMV term and the grid voltages, the upper and lower arm voltages with respect to the midpoint of the DC-Link-1 ("o") are derived into Eq.3.4 [11].

$$\begin{aligned} \frac{V_{DC-1}}{2} &= L_d \cdot \frac{d(i_{DC-1})}{dt} + r_d \cdot i_{DC-1} + V_{ua} + L_m \cdot \frac{d(i_{ua})}{dt} + ... \\ &... + r_m \cdot i_{ua} + L_{eq} \cdot \frac{d(i_{ga})}{dt} + r_{eq} \cdot i_{ga} + V_{ga} + V_{no} \\ \frac{V_{DC-1}}{2} &= L_d \cdot \frac{d(i_{DC-1})}{dt} + r_d \cdot i_{DC-1} + V_{la} + L_m \cdot \frac{d(i_{la})}{dt} + ... \\ &... + r_m \cdot i_{la} - L_{eq} \cdot \frac{d(i_{ga})}{dt} - r_{eq} \cdot i_{ga} - V_{ga} - V_{no} \\ L_{eq} &= L_f + L_g \\ r_{eq} &= r_f + r_g \end{aligned} \tag{3.4}$$

Rearranging Eq. 3.4 using Eq.3.3 & Eq.3.2 the three-phase AC grid currents, the DC-Link-1 current, and the three-phase AC-CC continuous-time models are represented in Eq.3.5 [7][11].

$$\begin{aligned} \frac{d(i_{gy})}{dt} &= \frac{1}{L_m + 2 \cdot L_{eq}} [V_{ly} - V_{uy} - 2 \cdot V_{no} \cdot U - 2 \cdot V_{gy} - (r_m + 2 \cdot r_{eq}) \cdot i_{gy}] \\ \frac{d(i_{DC-1})}{dt} &= \frac{1}{6 \cdot L_d + 2 \cdot L_m} [3 \cdot V_{DC-1} - \sum_{z=a,b,c} (V_{uz} + V_{lz}) - (6 \cdot r_d + 2 \cdot r_m) \cdot i_{DC-1}] \\ \frac{d(i_{zy})}{dt} &= \frac{1}{6 \cdot L_m} [\sum_{k=a,b,c} (V_{uk} + V_{lk}) - 3 \cdot (V_{uy} + V_{ly}) - 6 \cdot r_m \cdot i_{zy}] \\ V_{no} &= \frac{1}{6} \cdot \sum_{y=a,b,c} (V_{ly} - V_{uy}) \end{aligned} \tag{3.5}$$

where

$$U = \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix}; i_{gy} = \begin{bmatrix} i_{ga} \\ i_{gb} \\ i_{gc} \end{bmatrix}; i_{zy} = \begin{bmatrix} i_{za} \\ i_{zb} \\ i_{zc} \end{bmatrix}; V_{uy} = \begin{bmatrix} V_{ua} \\ V_{ub} \\ V_{uc} \end{bmatrix}; V_{ly} = \begin{bmatrix} V_{la} \\ V_{lb} \\ V_{lc} \end{bmatrix}; V_{gy} = \begin{bmatrix} V_{ga} \\ V_{gb} \\ V_{gc} \end{bmatrix}; \quad (3.6)$$

Using Euler's discretization method, the continous-time model of the MMC variables presented in Eq.3.5 can be derived into the discrete-time model for a one step prediction, which is depicted in Eq.3.7 [7]. The superscript m and p represent the measured and predicted quantities, respectively, and T_{sc} represents the converter's controller sampling time [7][9][11].

$$\begin{aligned} i^p_{gy}(k+1) &= \Gamma_{ot} \cdot [V^p_{ly}(k) - V^p_{uy}(k) - 2 \cdot V^p_{no}(k) \cdot U - 2 \cdot V^m_{gy}(k)] + \Phi_{ot} \cdot i^m_{gy}(k) \\ i^p_{DC-1}(k+1) &= \Gamma_{dt} \cdot [3 \cdot V^m_{DC-1}(k) - \sum_{y=a,b,c} (V^p_{uy}(k) + V^p_{ly}(k)] + \Phi_{dt} \cdot i^m_{DC-1}(k) \\ i^p_{zy}(k+1) &= \Gamma_{zt} \cdot [\sum_{y=a,b,c} (V^p_{uy}(k) + V^p_{ly}(k)) - 3 \cdot (V^p_{uy}(k) + V^p_{ly}(k))] + \Phi_{zt} \cdot i^m_{zy}(k) \\ V^p_{no}(k) &= \frac{1}{6} \cdot \sum_{y=a,b,c} (V^p_{ly}(k) - V^p_{uy}(k)) \end{aligned} \quad (3.7)$$

where

$$\begin{aligned} \Gamma_{ot} = \frac{T_{sc}}{L_m + 2 \cdot L_{eq}}; \Phi_{ot} = 1 - \frac{(r_m + 2 \cdot r_{eq}) \cdot T_{sc}}{L_m + 2 \cdot L_{eq}}; \\ \Gamma_{zt} = \frac{T_{sc}}{6 \cdot L_m}; \Phi_{zt} = 1 - \frac{6 \cdot r_m \cdot T_{sc}}{6 \cdot L_m} \\ \Gamma_{dt} = \frac{T_{sc}}{6 \cdot L_d + 2 \cdot L_m}; \Phi_{dt} = 1 - \frac{(6 \cdot r_d + 2 \cdot r_m) \cdot T_{sc}}{6 \cdot L_d + 2 \cdot L_m} \end{aligned} \quad (3.8)$$

It is evident from Eq.3.7 that the grid currents, the AC-CC, and the DC-Link-1 current components are decoupled, allowing them to be controlled independently. It's also important to note that the models presented are dependent on the predicted arm voltages, which are in turn reliant on the predicted SMs capacitor voltages. Thus, the HB-SM and arm discrete-time model are presented in the following subsection.

3.1.2 Modelling of the HB-SM and Arm Voltage

The HB-SM equivalent model is represented in Fig.3.2. Composed of two MOSFETS devices operated in a complementary manner, it is able to generate the voltage levels "0" and "V_c" at the output of the SM.

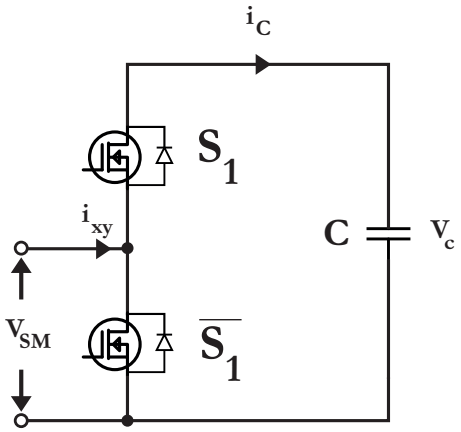


Figure 3.2: Equivalent model of HB-SM.

The continuous-time model of HB-SM capacitor voltage ,$V_c(t)$, is expressed through Eq.3.9. Where $V_c(0)$ represents the initial value of the capacitor voltage and i_c represents the current flowing through the capacitor. Taking into account that the controllers sampling time (T_{sc}) is very reduced, i_c is practically constant during one period. Thus the SM capacitor voltage is predicted for a one-step iteration through Eq.3.10, where i_c^p represents the predicted SM capacitor current, which is given in terms of measured arm current and respective switching state through Eq.3.11 [11].

$$V_c(t) = V_c(o) + \frac{1}{C}\int_{0+}^{t} i_c(\tau)\, d\tau \tag{3.9}$$

$$V_c^p(k) = V_c^m(k) + \frac{T_{sc}}{C} i_c^p(k) \tag{3.10}$$

$$i_c^p(k) = S_1 \cdot i_{xy}^m(k) \tag{3.11}$$

The predicted SM output voltage is represented through Eq.3.12 where V_{SM}^p represents the predicted SM output voltage, and V_c^m represents the measured SM capacitor voltage. Considering that each arm has N-SMs, their equivalent output voltage is expressed through Eq.3.13, where G_{xy} represents the arm voltage level, which is equivalent to the number of SMs to be inserted in an arm.

$$V_{SM}^p(k) = S_1 \cdot V_c^m(k) \tag{3.12}$$

$$V_{xy}^p(k) = \frac{G_{xy}(k)}{N} \sum_{h=1}^{N} V_{cxyh}^m(k) \tag{3.13}$$

3.2 DAB Converter

3.2.1 Steady-State Analysis

This section will go over the DAB converter's steady-state and power flow analysis. The AC link, which includes the energy transfer inductor (L_{DAB}) and high-frequency transformer, is powered by applying square-wave time-varying voltages, $V_{AC-1}(t)$ and $V_{AC-2}(t)$, to the HFT's terminal. The two full bridges are used to accomplish this. Each full bridge consists of two pairs of switching devices controlled by complementary square-wave pulses. The switching frequency of the converter (f_d) is the same as the switching frequency of these waves. In order to reduce the size of the inductances while enhancing the physical properties of SiC, HF switching will be used. The steady-state analysis can be simplified by taking into account the following assumptions [5]:

- All losses through the HFT's inductances are neglected;
- Parasitic capacitances and transformer magnetizing inductance, mentioned in Fig. 1.7. in chapter 1, are negligible due to the high frequency;
- Both full bridge circuits can be substituted by respective voltage sources V_{AC-1} and V_{AC-2}, which are applied to the terminals of the HFT;
- All secondary side quantities are referred to the primary side, which for the modelled system is the HVDC-link side;
- Constant supply voltages V_1 and V_2 are considered.

These assumptions lead to a lossless model of the DAB converter, which is represented in Fig.3.3, where the inductance L_k represents the inductance of the DAB converter, which is equal to the external inductor (L_{DAB}) plus the equivalent leakage inductance of the HFT's windings referred to the primary side. This quantity is expressed through Eq.3.14.

$$L_k = L_{DAB} + L_1 + n^2 \cdot L_2 \tag{3.14}$$

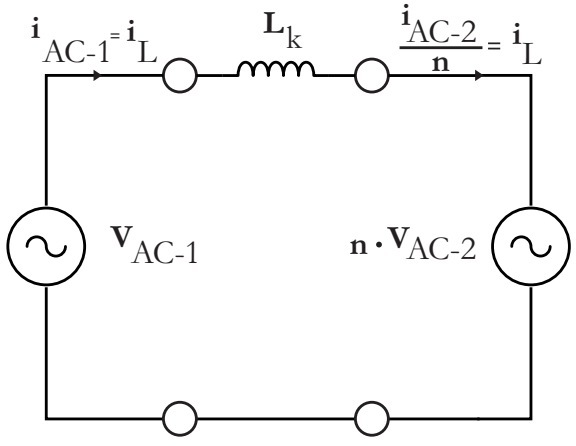


Figure 3.3: Lossless model of the DAB converter.

The equivalent voltage sources from the lossless model can produce three distinct voltage levels for the full bridge configuration shown in Fig. 2.3. Table 3.1 shows the switching states and their corresponding voltage levels for the high voltage side, denoted by V_{AC-1} [32].

Table 3.1: Full bridge switching states.

State	M_1	M_2	M_3	M_4	$V_{AC-1}(t)$
I	1	0	0	0	$+V_1$
II	1	0	1	0	0
III	0	1	0	1	0
IV	0	1	1	0	$-V_1$

Using the same analysis, the combination of switching states of $T_{5...8}$ results in secondary AC voltage, (V_{AC-2}) of $+V_2$, 0 or $-V_2$. Accordingly, the voltage across the inductor, $V_l(t)$ is defined through Eq.3.15. Consequently, the generated current through L_k at instant t_1 is depicted in Eq.3.16.

$$V_l(t) = V_{AC-1}(t) - n \cdot V_{AC-2}(t) \tag{3.15}$$

$$i_L(t_1) = i_L(t_0) + \frac{1}{L} \cdot \int_{t_0}^{t_1} V_l(t)\, dt \tag{3.16}$$

Having t_0<t_1 and an initial condition of $i_L(t_0)$ at t_0, the respective instantaneous power in each side of the converter is either generated or received by voltage sources V_{AC-1} and V_{AC-2} and is expressed in Eq.3.17. Considering an entire switching cycle $T_d = \frac{1}{f_d}$, the average power for both sides is calculated through Eq.3.18. Since a lossless model of the DAB was considered for the analysis the power flowing through both bridges must be equal, resulting in Eq.3.19.

$$\begin{aligned} p_1(t) &= V_{AC-1} \cdot i_L \\ p_2(t) &= V_{AC-2} \cdot i_L \end{aligned} \tag{3.17}$$

$$\begin{aligned} P_1 &= \frac{1}{T_d} \cdot \int_{t_0}^{t_0+T_d} p_1(t)\, dt \\ P_2 &= \frac{1}{T_d} \cdot \int_{t_0}^{t_0+T_d} p_2(t)\, dt \end{aligned} \tag{3.18}$$

$$P_1 = P_2 \tag{3.19}$$

Concluding the analysis, the converter's power level can be controlled through one or more of the following parameters:

- Switching frequency, f_d;
- Phase shift, φ between $V_{AC-1}(t)$ and $V_{AC2-}(t)$ (with $-\pi < \varphi < \pi$);
- Duty cycle, D, of the pulses applied at both bridges, with $0 < D < 0.5$.

Chapter 4

System Control

4.1 Control of the MMC

The usage of the MMC implies a complex control scheme as it brings several control objectives. Besides controlling the three-phase currents, the control scheme must ensure that inside variables to the MMC, such as SM capacitor voltage and minimization of CC, are maintained within the limit, preventing malfunction.

Classical control methods were developed to achieve multiple control objectives. These can be summarized into two categories, **open-loop** and **closed-loop** approaches [11] [6]:

- **Open-loop**: This approach uses the estimated energy in each arm, measured currents, and input voltage to choose the converter modulation indices.
- **Closed-loop**: Manipulate variables in the stationary (abc) frame, stationary ($\alpha - \beta$) frame or synchronous ($d - q$) frame to achieve the control objectives.

The MMC's classical control methods depend on controller gains and bandwidth, switching frequency, and the type of modulation scheme, making their design and implementation a complex process.

With the increased processing power, the Model Predictive Control (MPC) emerges as a powerful algorithm to control high-power drives, including the MMC. This approach avoids using Proportional-Integral (PI) controllers and pulse-width modulators, translating into an improved dynamic response and controllability [11]. This simple design algorithm is robust to system parameter variation, easily includes system constraints and nonlinearities, and compensates control delay.

This section explores the MMC converter's control, beginning with the control's objectives and moving on to a brief overview of the available MPC algorithms. Thereafter, an MPC algorithm is chosen and presented.

4.1.1 Control objectives

As mentioned before, the usage of an MMC implies achieving several control objectives besides the three-phase currents, other variables need to be controlled to ensure the safe and reliable operation of the converter. Each objective and its impact on the converter operation and performance are summarized in the following [28] [6] [11]:

- **Three-phase Currents:** The three-phase currents are controlled to meet the performance objectives of the converter depending on the application. For the studied case, a grid-connected system, the three-phase currents are controlled in order to meet the power factor requirement and desired power flow. This control objective is vital for the performance of the MMC.

- **SM Capacitor Voltage**: This control objective is crucial for the converter's power quality and reliability, and performance of three-phase current control. The control needs to maintain the average DC voltage of each leg to a value DC-Link-1 voltage, ensuring that this voltage is equally distributed throughout its arms and SMs.

- **Circulating Current**: The current components in each converter leg directly result from the potential difference between the arms. These pass through the converter's legs and have no effect on the AC side. However, incorrect CC control raises the effective value of the arm current, increasing the converter's losses and lowering its efficiency. Furthermore, if the CC current rises dramatically, the total current in one arm may exceed the rating of the semiconductor devices, compromising the converter's operation.

4.1.2 Model Predictive Control of MMC

The premise of MPC is to predict the system's behaviour and determine the appropriate switching state of the converter to fulfil the control objectives. To implement the method in digital platforms, the MPC requires a mathematical model of the MMC in the discrete-time domain, which is presented in chapter 3. It uses the discrete-time model to forecast the future behaviour of the control variables (r) for all possible switching states at sampling instant $(k+1)$. Furthermore, the results are compared to reference values using a cost function.[1] The cost function compares the reference values $(r^*(k))$ with projected control variables for each switching state. Each objective is optimized to achieve the required behaviour using a weighting factor that applies to all possible switching states. The function chooses the best state (S_{xyh}), and the cycle continues [6]. This procedure is illustrated in Fig.4.1.

[1] These can be extrapolated using Lagrange extrapolation or Vector Angle approaches (for perfect sinusoidal references), but it is not required for the procedure to properly work. [11]

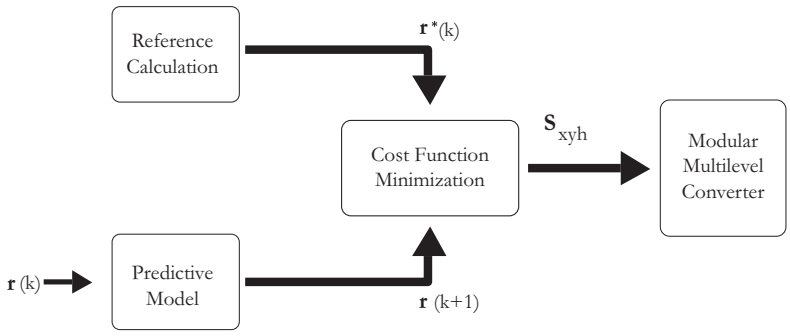


Figure 4.1: Block diagram of MPC.

Despite its popularity, the usage of an MPC has its challenges and issues:

- **Mathematical Modelling:** The technique is heavily reliant on the MMC's discrete-time model. The per-phase model is straightforward and computationally light. However, it fails to meet some of the control objectives, causing control variables to deteriorate [6]. As a result, it is not appropriate for all applications. Furthermore, three-phase modelling includes the CMV term by default, which reduces SM capacitor and DC-link-1 current ripple without evaluating them directly in the cost function [9].
- **Computational Burden:** With an increase in the number of SMs in each leg, the number of possible switching states increases dramatically. As a result of the increased computing load, the sample time increases. The MMC's steady-state performance is affected by a long sampling period [11]. Furthermore, the computational load varies depending on the cost function's control objectives.
- **Variable Switching Frequency:** When an MPC is used, the average SM switching frequency becomes dependent on the operating conditions, resulting in a variable harmonic profile and high switching power losses. The cost function can be used to control this variance. However, this has an impact on the performance of other control objectives [28].
- **Selection of Weighting Factors:** Multiple control objectives are included in the cost functions at the same time. The difference in weighting variables determines the relative relevance of one control target over another. As a result, a change in one objective's weighting component has a direct impact on the others. The MMC's performance is strongly influenced by the weighting factor, making its design one of the essential tasks in the MPC [6]. In the MPC, the per-unit technique can be used to calculate weighting factors. The heuristic method, however, is still the favoured method for acquiring the components [11].

4.1.2.1 Model Predictive Control Methodologies

There are different methodologies while implementing an MPC. These can be divided into categories, per-phase and three-phase, depending on the selected mathematical topology. While a per-phase based MPC requires three independent predictive algorithms to achieve all control ob-

jectives, a three-phase based MPC requires only one. Inside each category, different optimization principles to evaluate the cost function exist. Briefly, these can be summarized in the following:

- **Optimal Switching State (OSS) MPC (OSS-MPC):** This approach applies both for per-phase and three-phase modelling. It is the traditional MPC approach with no reduction of possible cases, consisting of a cost function that compares predicted control variables at $(k+1)th$ sampling instant (obtained with the discrete-time model of the converter) with extrapolated reference values. Each control objective is optimized by using a weighting factor, and the function selects an optimal switching state from all possible states. In the case of per-phase **OSS-MPC**, the cost function must include CC, three-phase currents and SMs capacitor voltage. Each phase has a computational burden of C_N^{2N}, leading to a total of $3 \cdot C_N^{2N}$, in the entirety of the converter [20]. On the other hand, in three-phased **OSS-MPC**, CC control is not mandatory up to a certain extent, and all the control objectives are included in a single cost function and evaluated for $2^{3 \cdot 2N}$. Even though the per-phase methodology has less computational burden, the three-phase has better dynamic/steady-state performance [6]. Moreover, the CMV term is included in the three-phase approach. This reduces the ripple in the DC-Link-1 current, as it blocks the zero-sequence CC entering the DC-Link-1 [9].

- **Optimal Voltage Level (OVL) MPC (OVL - MPC) & Optimal Switching Vector (OSV) MPC (OSV - MPC):** The problem with **OSS** philosophies is that they require a high number of switching states, which dramatically increases with the number of SMs, resulting in unrealistic computing demands for digital platforms as the sampling time increases. As a result, new techniques such as the **OVL** and **OSV** were created. The computational load is minimized by reducing the number of switching states through different strategies. Inevitably, the MMC's steady-state performance and power quality will degrade. When developing these approaches, the sample duration, the number of switching states, and the performance of the control objectives must all be taken into account. These algorithms use a predictive algorithm to optimize the cost function and determine the best **OVL** or **OSV**, depending on the mathematical model used to regulate the converter, per-phase or three-phase, respectively. The **OVL** or **OSV** represents the number of "ON" state SMs in each arm. This data is then given to a sorting and logic-based voltage balance algorithm, which inserts selective SMs out of N-SMs in each arm depending on the **OVL/OSV**, SM capacitor voltage, and arm current direction [11]. The OVL-MPC requires evaluating $(N+1)$ voltage levels per phase leading to a total of $3 \cdot (N+1)$ levels for a three-phase system. The **OSV-MPC** method, on the other hand, necessitates the evaluation of $(N+1)^3$ switching vectors [8]. The **OSV-MPC** has a higher computational complexity in general. It does, however, provide higher steady-state performance and power quality due to the three-phase modelling [6].

- **Dual-Stage MPC:** Implementing the predictive algorithm in various phases, combining the concept of **OSV-MPC** and **OSS-MPC** techniques, is another way to lessen the three-phase **OSS-MPC** computational burden. A two-stage predictive algorithm is used to attain the

overall goals. In **Stage-I**, a single cost function is provided with calculated references to meet the desired objectives. This function is optimized to find the **OSV** from all of the $(N+1)^3$ switching vectors. Each switching vector is given to the predictive **Stage-II** and indicates the required number of inserted SMs in each arm. **Stage-II** is intended to maintain the voltage of the SM capacitors at their reference value. It predicts the voltage of SM capacitors using a discrete-time model of the SM capacitor. The reference and real SM capacitor voltages are then used to create a cost function. For all potential switching states corresponding to the **OSV**, the resultant cost function is evaluated. The **OSS** is then chosen and applied to the converter [7]. This method is simple to apply and enhances dynamic performance while eliminating the usage of traditional voltage balance methods. **Stage-I** needs to evaluate $(N+1)^3$ state while **Stage-II** considers $C^N_{N/2}$ if N is even and $C^N_{(N+1)/2}$ if N is odd [6].

When comparing the different philosophies, the three-phase **OSS-MPC**, **OSV-MPC**, and **dual-stage MPC** techniques outperform the per-phase **OSS-MPC** and **OVL**-approaches in terms of steady-state performance. This is related to the previously indicated three-phase mathematical modelling. Because of the single-stage predictive algorithm, which controls all control objectives through a single cost function, the **OSS-MPC** strategies offer the best dynamic responsiveness. The **OVL-MPC** and **OSV-MPC**, on the other hand, use a first predictive stage and a classical voltage balancing algorithm in the posterior. Despite this, the **dual-stage MPC** has a faster dynamic response than the previous two due to the lack of a sorting algorithm. Nevertheless, these strategies must also be compared in terms of switching states evaluated in the cost function, which directly influences the computational burden, which is limited by the digital platform. It is noticeable that the **OSS-MPC** approaches have the highest computational burden of all, whereas the **OVL-MPC** has the least.

Considering that the system proposed is grid-connected, to avoid grid disturbances and preserve power quality, three-phase mathematical modelling is obligatory, directly excluding **OSS-MPC** (per-Phase) and **OLV-MPC** approach. A fast dynamic response is also desirable, discarding the **OSV-MPC**. Moreover, when comparing the computational burden, the **dual-stage MPC** wins over the **OSS-MPC** (three-phase) as the number of switching states is drastically reduced. Thus, the chosen approach to control the converter employed in the first stage is the **dual-stage MPC**.

4.1.3 Dual-Stage MPC

As the name implies, the chosen **MPC** approach for regulating the MMC converter is divided into two parts. There are two types of control objectives, primary and secondary. The primary group consists of three-phase currents and CC, whereas the secondary group consists of the SMs capacitor voltage. In **Stage-I**, the control objectives are evaluated for a total of $(N+1)^3$ switching vectors (where N denotes the number of SMs per arm). Each switching vector represents the number of SMs injected in each of the three stages. The **OSV** is calculated using a cost function, and the results are sent to the **MPC Stage-II**. The SMs capacitors voltages are predicted and included in a cost function. This function is evaluated for all switching states corresponding to the **OSV**

provided. The converter is switched to the switching state that minimizes the cost function.

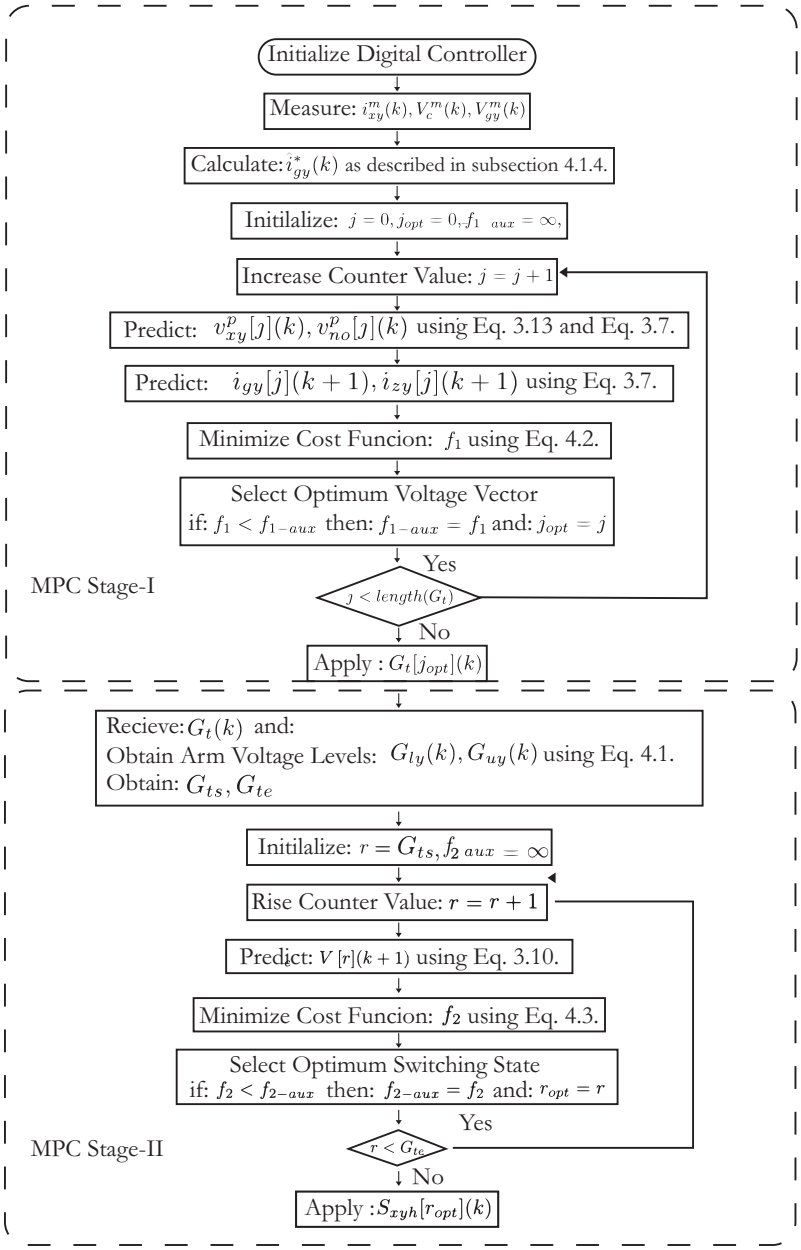


Figure 4.2: Flowchart of the dual-stage MPC.

The flow chart of the **dual-stage MPC** scheme is shown in Fig.4.2. The algorithm involves 5 major steps, which are explored below [7]:

1. **Measurement and Synthesis of Feedback Signals:** Measurement of the upper (i^m_{yu}) and lower arm (i^m_{yl}) currents, SM capacitors voltage (V^m_{cxyh}), and three-phase grid voltages (V^m_{gy}). The three-phase grid currents (i_{gy}), CC (i_{zy}) and DC-Link-1 current (i_{DC-1}), are obtained from Eq.3.3, and Eq.3.2 respectively.

2. **Calculation of three-phase Reference Currents:** The three-phase reference currents are

generated with a required magnitude and frequency. This process varies according to the application. In the case of grid-connected systems, the reference currents are obtained from the active and reactive power demands. In subsection 4.1.4, this procedure is further explored.

3. **Prediction of Future Behaviour of MMC:** Making use of the discrete-time model of the converter with the measured quantities and systems parameters, the future behaviour of the grid currents ($i_{gy}(k+1)$) and the CCs ($i_{zy}(k+1)$) are predicted through Eq.3.7. These variables have to be calculated for every single voltage vector (G_t). Each voltage vector consists of three elements representing the lower arms voltage levels of the three phases. The number of upper arms voltage levels is obtained by subtracting the lower arms voltages levels from the total number of SMs per arm (N):

$$\begin{aligned} G_{ly}(k) &= G_t(k) \\ G_{uy}(k) &= N - G_t(k) \end{aligned} \tag{4.1}$$

This relation allows for a drastic reduction of the computational burden. Finally, the predicted arm voltages $v^p_{xy}(k)$ are obtained through Eq.3.13, and used in the discrete-time model of the converter.

4. **Minimization of Cost Function - Stage-I:** The grid currents references ($i^*_{gy}(k)$) and predicted grid currents ($i^p_x(k+1)$), as well as the reference (i^*_{zy}[2]) and predicted CCs ($i^p_{zy}(k+1)$), are included in a cost function which is given by:

$$f_1(k) = \lambda_0 \cdot |i^*_{gy}(k) - i^p_{gy}(k+1)| + \lambda_1 \cdot |i^*_{zy} - i^p_{zy}(k)| \tag{4.2}$$

where λ_0 and λ_1 are the weighting factors, these parameters set the relative importance of one control objective over the other. The function (f_1) is evaluated for a total of $(N+1)^3$ converter voltage vectors. For each voltage vector, the predicted grid currents and predicted CCs are compared with the reference currents. The voltage vector which minimizes the cost function (f_1) is selected and applied to **Stage-II** of the MPC.

5. **Minimization of Cost Function - Stage-II:** Once the **OSV** is found, the information is provided to **Stage-II**. The SM capacitors voltages are predicted using Eq.3.10. The predicted (V^p_{cxyh}) and reference SM capacitors voltages (V^*_c[3]) of each phase are included in a cost function as shown by:

$$f_2(k) = \lambda_v \cdot |V^*_c - V^p_{cxyh}| \tag{4.3}$$

In this case, since the control objective is solely one, the weighting factor, λ_v, is set to 1. The cost function (f_2) is evaluated for all switching states corresponding to the required arm voltage level (G_{xy}) provided from **Stage-I**. The switching state (S_{xyh}) which minimizes the cost function is selected and applied to the converter.

[2] As the CCs want to be minimized, the reference (i^*_{zy})), is set to zero.
[3] The reference SM capacitors voltages is set to V_{DC-1}/N.

4.1.4 Reference Current Generation

The dual-stage MPC, which ensures that all three primary control objectives are met, was discussed in the preceding subsection. However, the double step prediction algorithm main function is to follow grid current references, not to calculate them. To calculate these, an external control mechanism is required.

The grid current references calculation plays the most important role in satisfying grid requirements, as these define the grid's active and reactive power flow. In the examined application, a closed-loop technique is used to keep the DC-Link-1 around its reference value. The controller's block diagram is shown in Fig. 4.3.

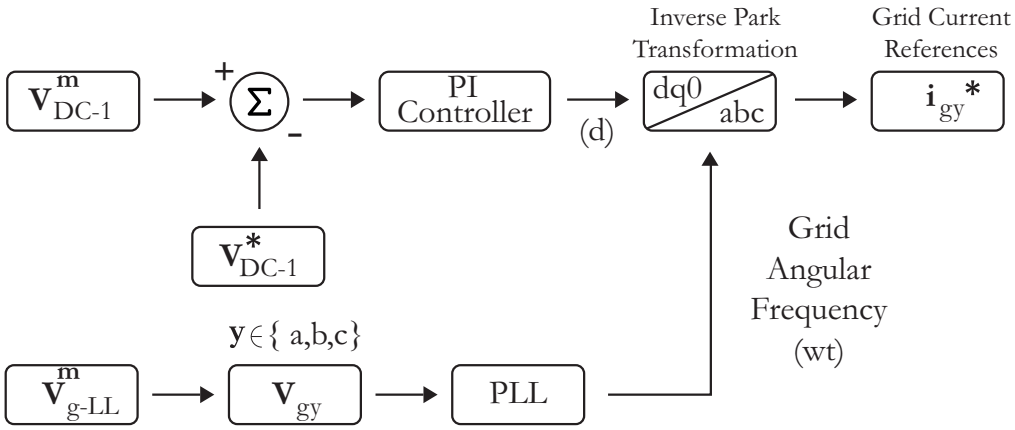


Figure 4.3: Representative diagram of the grid current references calculation.

The active and reactive components of grid currents are decoupled using this control approach. A conversion to the synchronous frame ($d - q$) is required for this. The active power flow is controlled by component d. Component q, on the other hand, controls the reactive. The program was created with a power factor of unity ($I_q = 0$). However, alternative approaches for regulating reactive power to satisfy grid requirements could be used.

Since the goal is to control the voltage in the DC-link-1, a voltage error signal is fed to a PI controller. The controller's output is then fed to the d component of the $dq - abc$ block. The tuning of the PI controller is crucial to achieve optimal transient response and minimize steady-state error. Thus, the active current controls the DC-Link-1 voltage, either for power consumption or power injection to the AC grid.

In addition, a Phase-Locked-Loop (PLL), is needed to "track" the grid angular frequency. It does this by synchronizing on zero crossings of phase a's positive-sequence [4]. The grid's angular frequency is supplied to the $dq - abc$ transformation block, which uses the inverse park transform to give the MPC algorithm the grid reference currents in the abc-frame.

4.2 Control of DAB

4.2.1 Phase Shift Modulation

The phase shift modulation technique is the most commonly utilized modulation technique in DAB converter applications. There are several variations on this approach, the simplest of which is the Single-Phase Shift (SPS). The primary premise is to regulate all switches in the converter's two full bridges with a constant switching frequency and a maximum duty cycle of 50%. It is possible to regulate the amount of power transferred between the primary and secondary bridges by varying the phase shift angle (φ) between the primary and secondary bridges [16]. Furthermore, as the phase shift ratio between the applied square waves to both bridges increases, a voltage differential is formed across the leakage inductance of the transformer, charging and discharging it and thereby channeling its stored energy. The power flow direction depends on the signal of the phase shift. The positive shift angle is defined when the primary voltage leads the secondary voltage since the energy flows from the primary side to the secondary side [15]. This concept is illustrated in Fig.4.4 through the DAB's waveforms.

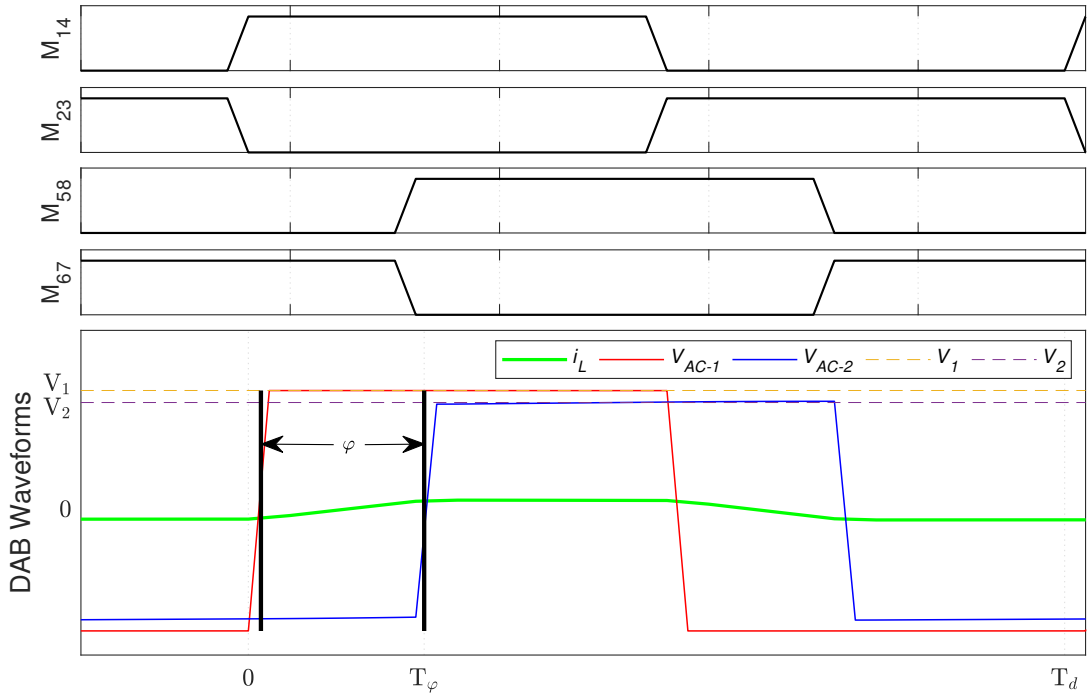


Figure 4.4: Drive signal and corresponding current and voltage waveforms in the DAB with the SPS control.

To better understand the SPS control method, the following analysis based on references [5] [15] [16] is provided. Analyzing Fig. 4.4, during a full cycle T_d, supply voltages V_1 and V_2 are kept constant, as is the phase shift time interval T_φ. Thus, the voltages $V_{AC-1}(t)$ and $V_{AC-2}(t)$, as well as the inductor current i_L, repeat with their symmetric value every half-cycle. Accordingly

the definitions depicted in Eq.4.4 are formulated.

$$\begin{aligned} V_{AC-1}(t + T_d/2) &= -V_{AC-1}(t),\ with\ V_{AC-1}(t) = \pm V_1 \\ V_{AC-2}(t + T_d/2) &= -V_{AC-2}(t),\ with\ V_{AC-2}(t) = \pm V_2 \\ i_L(t + T_d/2) &= -i_L(t) \end{aligned} \tag{4.4}$$

The symmetry of the current waveform (I_L) through the leakage inductance allows for the power flow analysis to be developed for only half a switching cycle ($\frac{T_d}{2}$). Considering $t_0 = 0$ and definitions made on 4.4, the transferred power is described through Eq.4.5. Moreover, in order to derive an analytical expression for the transferred power (P), the inductor's current ($i_L(t)$) must be calculated, hence Eq.4.6 is defined.

$$P_1 = \frac{1}{T_d} \cdot \int_0^{T_d} p_1(t)\ dt = \frac{2}{T_d} \cdot \int_0^{T_d/2} V_{AC-1}(t) \cdot i_L(t)\ dt = \frac{2 \cdot V_1}{T_d} \cdot \int_0^{T_d/2} i_L(t)\ dt \tag{4.5}$$

$$\frac{d(i_L(t))}{dt} = \frac{V_{AC-1}(t) - V_{AC-2}(t)}{L} \tag{4.6}$$

Furthermore, for each half-cycle ($0 < t < T_d/2$) two separate time intervals I and II may be distinguished by analyzing the waveform of $i_L(t)$ in Fig. 4.4. Assuming $i_{L,0} = i_L(t_0)$ for steady-state operation and the definitions made on 4.4, the inductor current can be defined through Eq. 4.7, using solely a positive phase shift ($0 < \varphi < \pi$) for both the intervals.

$$\begin{aligned} time\ interval\ I:\ i_L(t) &= i_{L,0} + \frac{(V_1 + n \cdot V_2) \cdot t}{L}, \qquad \forall\ 0 < t < T_\varphi \\ time\ interval\ II:\ i_L(t) &= i_L(T_\varphi) + \frac{(V_1 - n \cdot V_2) \cdot (t - t_\varphi)}{L}, \qquad \forall\ T_\varphi < t < T_d/2 \end{aligned} \tag{4.7}$$

Taking into account the reversed-signs repetition identified in Eq.4.4 and considering $T_\varphi = \varphi/(2\pi \cdot f_d)$. The inductor current for $t = t_0$ is expressed through Eq. 4.8. Moreover, considering a lossless converter (Eq. 3.19) and the transferred power during a half-cycle (Eq.4.5), the transferred power is calculated for the entire phase shift range through Eq. 4.9.

$$i_{L_0} = \frac{\pi \cdot (n \cdot V_2 - V_1) - 2 \cdot \varphi \cdot n \cdot V_2}{4 \cdot \pi \cdot f_d \cdot L}, \qquad for\ 0 < \varphi < \pi \tag{4.8}$$

$$P = P_1 = P_2 = \frac{n \cdot V_1 \cdot V_2 \cdot \varphi \cdot (\pi - |\varphi|)}{2 \cdot \pi^2 \cdot f_d \cdot L}, \qquad \forall\ -\pi < \varphi < \pi \tag{4.9}$$

This expression shows a relationship between the power delivered from one side to the other as a function of the phase shift between the two bridges, the converter's switching frequency and the

energy transfer inductance. Moreover, Eq. 4.9 expresses the operating modes of the converter. The transferred power is positive for a positive phase shift, which translates into buck mode operation - power transferred from the high voltage bridge to the lower voltage bridge. On the other hand, when the phase shift is negative, the transferred power is negative, translating into boost mode operation - power transferred from the low voltage bridge to the higher voltage bridge. Analyzing Eq.4.9, maximum power transfer occurs for $\varphi = \pm\pi$. Thus the maximum transferred power is expressed through Eq. 4.10. Finally, Eq.4.9 can be rewritten to obtain a specific value of φ to achieve a specific power, leading to Eq. 4.11.

$$|P_{max}| = \frac{n \cdot V_1 \cdot V_2}{8 \cdot f_d \cdot L}, \qquad for\ \varphi = \pm\pi/2 \tag{4.10}$$

$$\varphi = \frac{\pi}{2} \cdot \left[1 - \sqrt{1 - \frac{8 \cdot f_d \cdot L \cdot |P|}{n \cdot V_1 \cdot V_2}}\right] \cdot sgn(P), \qquad \forall\ |P| < |P_{max}| \tag{4.11}$$

The single-phase shift method is by far the most straightforward method to manage the DAB converter. However, this control mechanism only has one control degree of freedom because the power transfer is only related to the phase shift angle φ. This leads to a small voltage range for optimal performance, namely attaining ZVS, which minimizes switching losses dramatically [32]. Furthermore, a higher CC, often referred to as reactive power, is expected, resulting into higher RMS current increases, resulting in increased power losses [16].

4.2.2 Phase Shift Voltage Loop

Having the analysis on the SPS control method made, it is now necessary to describe how the phase shift between the square waves is generated. Since the SST application is designed to integrate a BSS to the electrical grid, the system must be able to maintain voltage stability despite the different charging or discharging regimes, plus able to supply loads on both DC-links. Thus, the phase shift between the waves applied to the DAB converters of second stage is obtained through the voltage loop represented in Fig.4.5. Making a closer analysis, the measured DC-Link-2 voltage (V^m_{DC-2}) is subtracted by the reference DC-Link-2 voltage (V^*_{DC-2}) generating an error signal. This error signal is applied to a PI controller to generate the desired phase shift (φ) between the waves. Two square waves with a duty cycle of 0.5 are then generated using PWM with a sawtooth wave serving as reference signal, which dictates the DAB converters switching frequency (f_d). Depending whether the SST is charging or discharging the battery pack, the phase-shift can be either positive or negative. Positive for charging (buck-mode operation) and negative for discharging the battery pack and supply energy to the grid (boost-mode operation). Depending on the SST's operation mode the controller defines a positive or negative gain for the phase shift (φ).

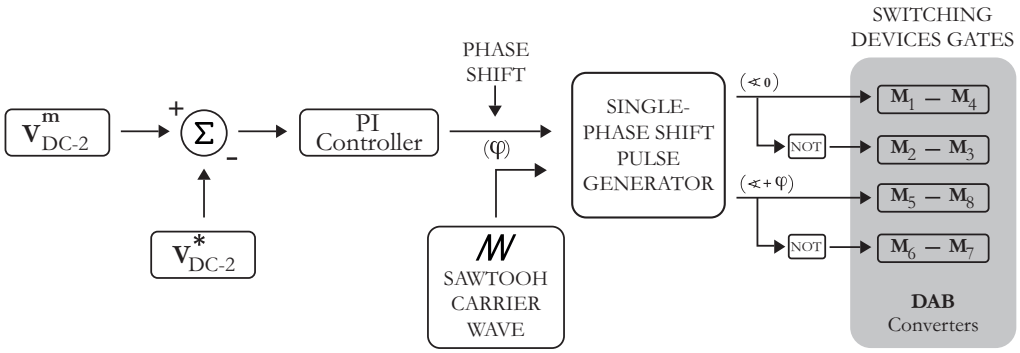


Figure 4.5: Representative diagram of DC-Link-2 voltage loop for DAB converter control.

4.3 Control of DC-DC converter

As mentioned before, the DC-DC converter employed in the BSS needs to be able to control the battery pack current (i_{BAT}) in order to correctly charge and discharge the pack. A simple control method, which is represented in Fig.4.6, was designed to control the two switching devices of the converter. As mentioned before, only current control was developed. For this, the measured battery pack current (i^{m}_{BAT}) is subtracted by the reference current (i^{*}_{BAT}) generating an error signal. This error signal is applied to a PI controller, which generates the desired duty-cycle for a PWM signal. This duty-cycle is applied to a PWM generator which generates the switching pulses for T_1. The switching pulses for T_2 are obtained by negation of T_1.

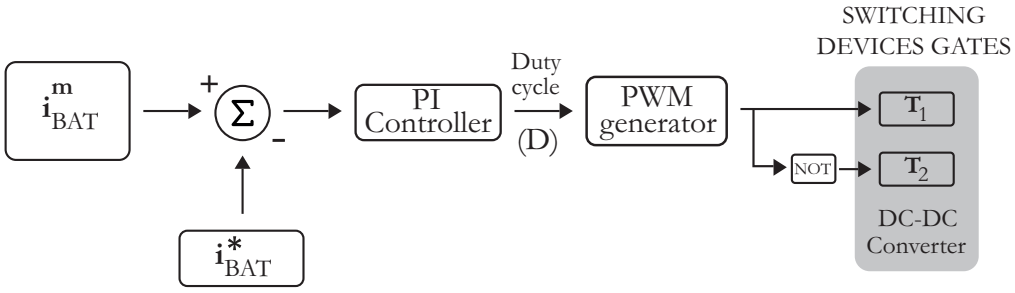


Figure 4.6: Representative diagram of battery pack current loop for DC-DC converter control.

Chapter 5

Simulation Results

To validate the performance of the proposed system and its associated control techniques, a simulation study was undertaken using MATLAB/Simulink. All simulation were conducted with a sampling time of $T_s = 5\mu$s. The system's nominal power is 1kW, and the rated grid line-to-line voltage, V_{ll}, is 100V. The MMC connects the DC-link-1, which has a rated voltage of 200V, to the electrical grid. Two HB-SMs are used in each arm of the converter to evenly distribute the 200V between the SMs capacitors. As a result, each SM has a 100V rated capacitor. The dual-stage MPC algorithm has a sampling control time of $T_{sc} = 70\mu$s. The DC-Link-1 comprises of capacitor and a variable DC-Load. The DC-Link-1 connects to the second conversion stage.

The second conversion stage comprises of two DAB converters connected in an ISOP topology, which are connected to the DC-link-1. The DC-link-1 voltage is shared in series by the two converters. As a result, the primary side voltage of the converters is rated at 100V, while the power voltage is transformed to 90V on the secondary side and shared in parallel by the converters in order to reduce the secondary winding currents of the DABs. The secondary side of the DAB converters is the DC-link-2 where a capacitor is used to regulate the voltage. Different load regimes are imposed to study the converters performance, and finally a battery storage system is employed to verify the system's bidirectional capabilities. Tab.7.1 lists the system parameters used in the simulation. The sections that follow will detail multiple experiments with various conditions imposed on the system with the scope of testing its performance.

5.1 First Conversion Stage

5.1.1 Steady-State Performance Analysis

The system was set to run around its nominal power with a load of 40 Ω in DC-link-1 to analyze the steady-state performance of the first conversion stage, even though the system is drawing more than 1 kW because the two conversion steps require a fraction of the power to function which translates into losses, hence the grid current has an RMS value slightly higher than its nominal value stated in Table 7.1. The grid voltage waveforms of a direct three-phase system with unaccessible

ground are shown in Fig. 5.1 (a). In addition, the grid currents are shown in Fig. 5.1 (b), and they are in phase with the grid voltages since the reference currents are generated using a PLL that tracks the angular frequency of the grid voltages and feeds it into the reference current calculation, which is part of the DC-Link-1 voltage control scheme explained in section 4.1.4, Fig. 4.3. It is statable that the MPC algorithm is able to perfectly control the three-phase currents as the display a sinusoidal shape with a minor THD of only 2.25%. Furthermore, looking at (c), it is clear that the converter can control the DC-Link-1 voltage because the voltage ripple is around 0.5V, and the DC-Link-1 current has a modest ripple of 0.7A.

Using a CC gain of 0.8 (λ_1, used in MPC cost function 1 presented in Eq. 4.2), which was determined empirically to be the best value for the converter's good performance, it is possible to analyze the well functioning of the MPC algorithm and the performance of the rest of its control objectives. When looking at Fig. 5.2 (a), it is statable that the arm currents are balanced in nature and related to the grid currents through Eq. 3.3. It is apparent that the arm currents are around 50% of the grid current peaks, which is desirable, since it keeps the arms RMS current value low and reduces the converter's losses.

Furthermore, it is clear from Fig. 5.2 (b) that the cost function utilized in stage-I described in Eq. 4.2 is minimizing CCs as it should be, as these only reach a peak of 1 A. The double frequency of CCs anticipated by mathematical modelling can also be verified. Finally, the voltage waveforms of the SMs in phase-a are shown in Fig. 5.2 (c). Because their ripple reaches a maximum of 5V, it is foreseeable that they will maintain their value around the reference. Thus, the prediction stage-II, described in Chapter 4, is working properly.

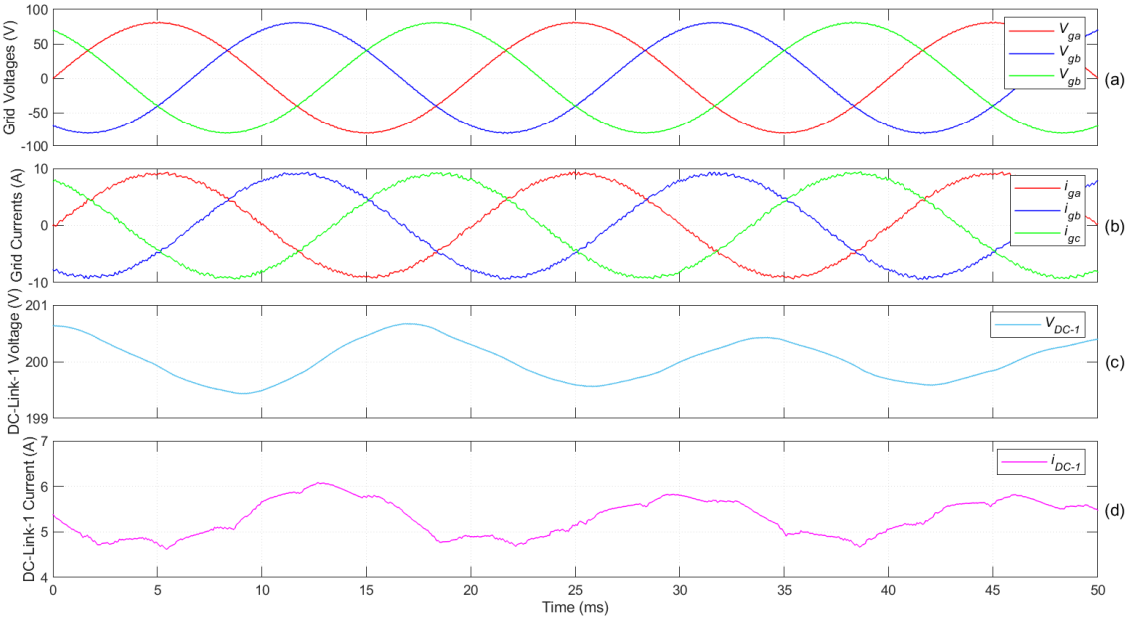


Figure 5.1: First stage steady-state performance: (a) Grid voltages. (b) Grid currents. (c) DC-Link-1 Voltage. (d) DC-Link-1 Current.

Analyzing the converter's input line-to-line voltage, V_{ab}, shown in Fig. 5.3 (a), it can be seen

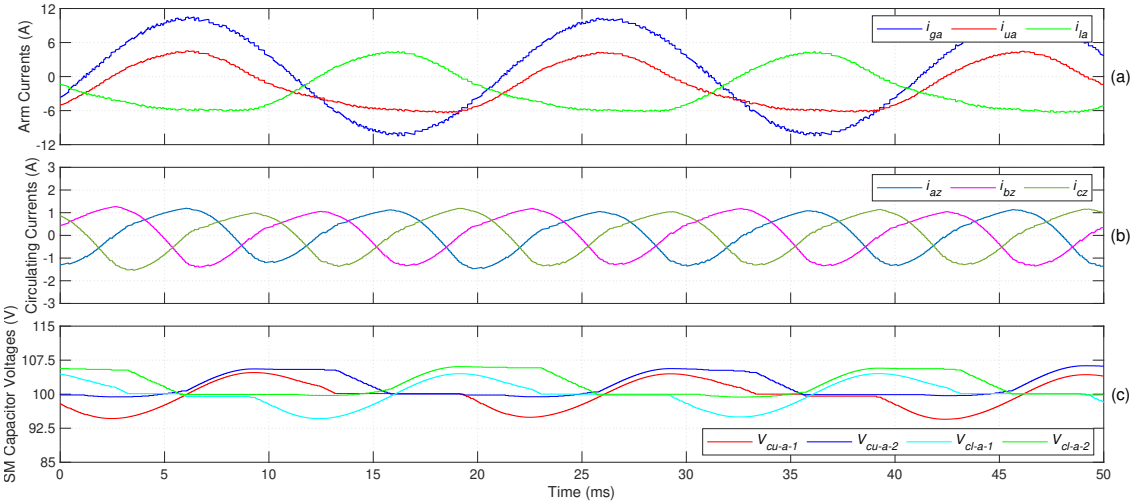


Figure 5.2: MMC steady-state performance: (a) Arm Currents phase-a. (b) Circulating currents all phases. (c) SMs Capacitor voltages, phase-a.

that the waveform increases in steps of 100V, in a sinusoidal-like shape, with a maximum peak value of 200V. This makes sense, considering that the converter must regulate each phase voltage in order to control grid currents precisely. The CMV term, shown in Fig. 5.3 (b), and described by Eq. 3.5, is incorporated in the mathematical modelling of the converter and reduces the THD value of V_{ab} to 31.22%. Furthermore, because the CMV term has a peak voltage of 65V, it can be used to reduce switching frequency, SM capacitor voltage ripple, and the amount of CCs by blocking zero-sequence CCs and thereby lowering the DC-Link-1 current. As a result, the system's steady-state performance is good.

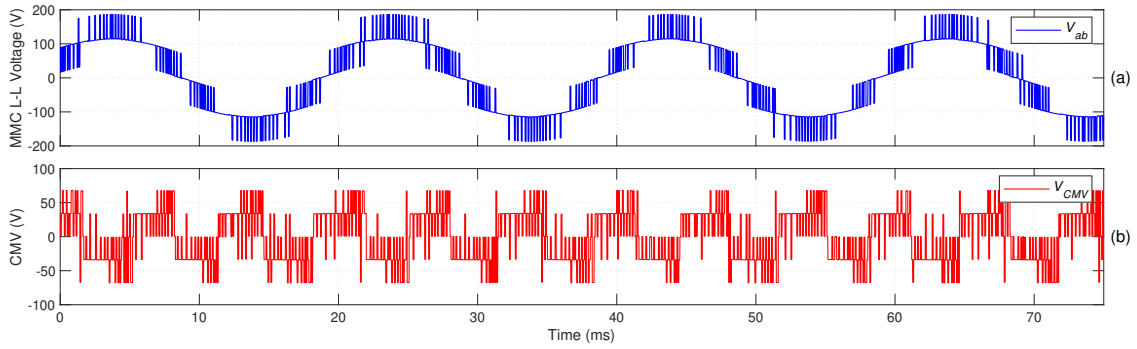


Figure 5.3: MMC steady-state performance: (a) Line-to-line voltage. (b) Common-mode voltage.

5.1.1.1 Circulating Current Control Turned Off

The same tests were run with a CC gain of zero ($\lambda_1 = 0$), with the goal of assessing the impact of CCs on system performance. The MMC voltage waveforms are depicted in Fig. 5.4, and Table 5.1 compares key system parameters to better quantify the system's performance in relation to the CCs control.

Table 5.1: First stage performance values with and without CC control.

λ_1	$V_{DC-1-Ripple}(V)$	$i_{DC-1-Ripple}(A)$	$V_{ab-THD}(\%)$	$I_{g-THD}(\%)$	$AVG\ I_{grid-RMS}(A)$	$AVG\ I_{arms-RMS}(A)$	$AVG\ I_{circ-RMS}(A)$
0.8	0.5	0.7	31.22	2.25	6.599	3.825	0.79
0	0.5	0.75	30.5	2.18	6.692	4.428	2.758

The arm current waveforms, as shown in Fig. 5.4 (a), are no longer balanced; however, the grid currents maintain a perfectly sinusoidal waveform with a THD of 2.18%, as these are the only objective considered in the MPC-Stage 1, and thus the average value of three-phase grid currents is left unchanged, as shown in Table.5.1. The CCs, like the arm currents, have an unbalanced shape and, naturally, a higher RMS value because their control was set to 0 ($\lambda_1 = 0$) in Eq. 4.2 of the MPC stage-I. Table 5.1 shows the average of the three-phase CCs for both scenarios; naturally, with $\lambda_1 = 0$ the average three-phase CCs RMS value is increased by about 2A.

Consequently, this has an impact on the RMS value of the arm currents, with the lower arm current reaching a peak value of 9A at $t = 24$ms, almost the same as the grid current 10A, resulting in a 0.6A rise in the average RMS value of the three-phase arm currents. Furthermore, when the same analysis is performed on the SM's capacitor voltages, it is clear that the voltage ripple has risen, with V_{cl-1} dipping below 90V at $t = 30$ms, resulting in a ripple of more than 10%.

Finally, while looking at the first stage conversion performance through Table 5.1, the DC-Link-1 voltage remains unchanged while the DC-Link-1 current's ripple is increased by 0.05A. This makes sense because CCs have no effect on grid current control, hence the converter's ability to draw power from the grid while keeping the DC-link-1 voltage around its nominal value is unaffected. Nonetheless, because its interaction with CCs is described through Eq. 3.2 and Eq. 3.3, the DC-link-1 current ripple is influenced, having its value increased by 0.5A.

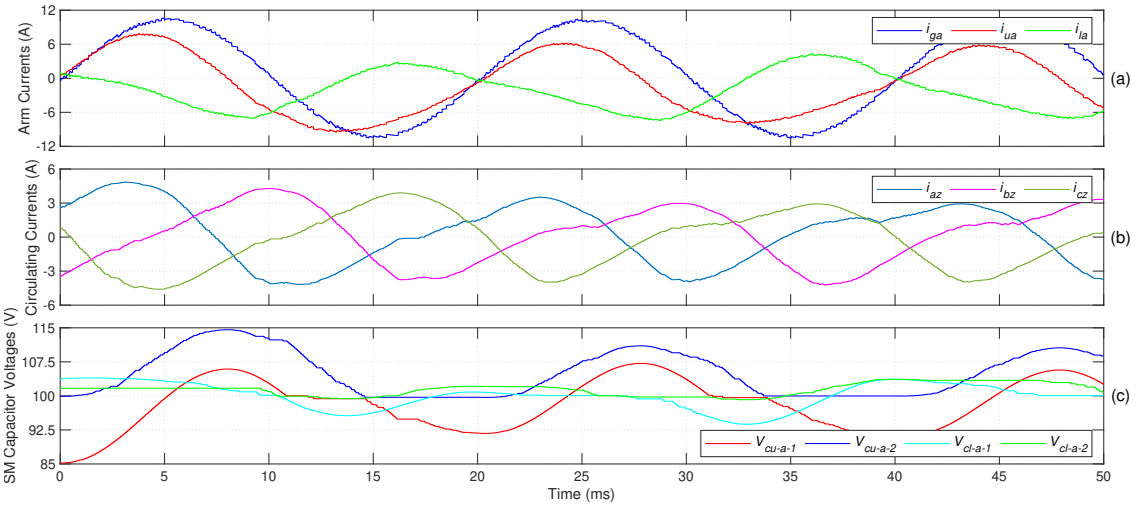


Figure 5.4: MMC steady-state performance (with $\lambda_1 = 0$): (a) Arm Currents phase-a. (b) Circulating currents all phases. (c) SMs Capacitor voltages, phase-a.

5.1.2 Dynamic Performance Analysis

With the purpose of testing the dynamic performance of the first conversion stage, load variations on the DC-Link-1 were imposed using Simulink's stair generator. The simulation begins with a DC-Link-1 load (R_{DC-1}) of 80Ω. The load is increased to 57.15Ω at $t = 0.5$s. As a result, the DC-Link-1 voltage, as shown in Fig. 5.5 (b), reduces by around 6V. However, because of the voltage loop control described in section 4.1.4, the PI controller that regulates the d component of grid currents responds quickly, increasing the grid reference shown by the blue-dotted line in Fig. 5.5 (a). The converter can swiftly follow this reference thanks to the dual-stage MPC, resulting in larger grid currents as shown in Fig. 5.5 (a). The input power of the converter grows as it follows the grid current reference, and the DC-Link-1 voltage is rapidly restored to its reference value in less than half a second. Furthermore, the DC-Link-1 current increases when the value of the R_{DC_1} drops, as seen in Fig. 5.5 (c), which is clearly explained by Ohm's law. The same operation is performed at $t = 1.5$s, but this time with $R_{DC-1} = 40\Omega$, forcing the system to operate at its nominal power. The system reacts in a similar way to the first test and is able to handle the load variation. Finally, the system was subjected to a load decrease test, with R_{DC-1} returning to its original value of 80Ω at $t = 2.5$s. As a result, the voltage on DC-link-1 has increased by about 20V. The voltage loop control detects this and lowers the grid reference current value, allowing the system to consume less power from the grid. This voltage variation is greater than all other load variations, resulting in a larger DC-link-1 current ripple. This response is stated clearly by the discretization model of i_{DC-1} stated by Eq. 3.7, which states the relationship between the i_{DC-1} and V_{DC-1}. Despite this, the system adapts fast, returning to its original steady-state in less than 1s.

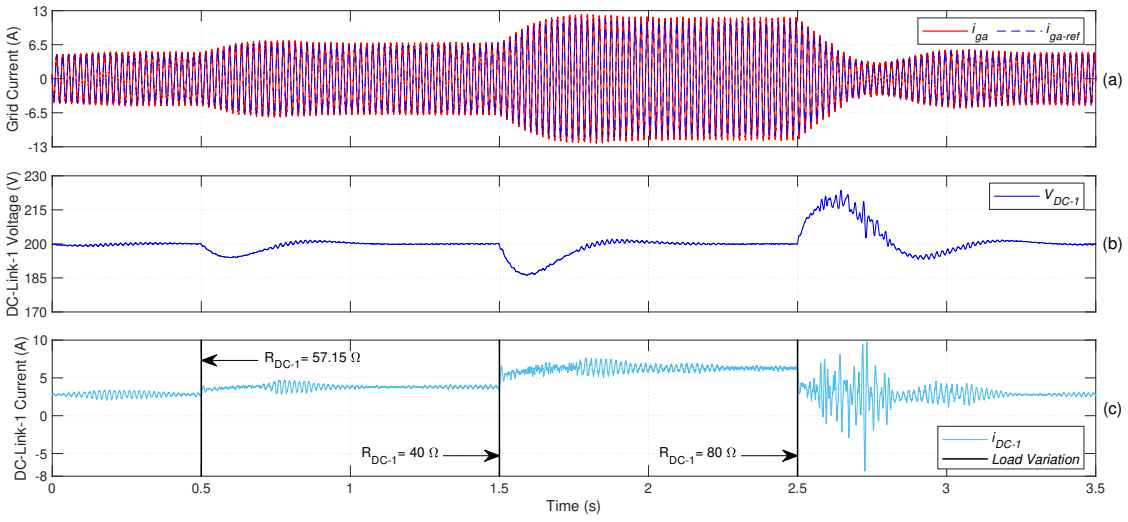


Figure 5.5: First stage dynamic performance: (a) Grid currents. (b) DC-Link-1 Voltage. (c) DC-Link-1 Current.

The waveforms of the converter's inner variables during the same dynamic test mentioned above are shown in Fig. 5.6 for the purpose of examining the MMC dynamic performance. Starting with the arm currents, shown in Fig. 5.6 (a), it is clear that the arm currents maintain a balanced

character throughout the test, assuming a lower value than the grid current, which is desired since it reduces the converter's losses and increases its efficiency. This is due to the CC regulation, which is part of stage-I of the dual-stage MPC and is carried out by the cost function 1 described in Eq. 4.2. When looking at the converter's CCs, as shown in Fig. 5.6 (b), it's clear that they're being minimized successfully, maintaining a low value during the test, and increasing in step with the grid currents, as explained by the mathematical relationship described in Eq. 3.1. Lastly, the SMs capacitor voltages maintain a value around their reference of 100V, indicating that stage-II of the MPC algorithm is working well. The discretization model of the SM capacitor voltage, given by Eq. 3.10, explains why the SMs capacitor voltage ripple is proportional to the arm currents.

Furthermore, when examining the transients, it is statable that the system handles the first two transients more efficiently than the third, due to the larger DC-Link-1 voltage fluctuation of 20V for $t = 2.5$s. This disturbance propagates throughout the converter, as each arm shares the entire DC-Link-1 voltage, the SMs capacitor voltages also increase at the given instant. Since the CCs are reliant on the arms voltages, they assume unbalanced waveforms and increased values, this relationship is given by Eq. 3.5. Moreover, the arm current waveforms are also unbalanced throughout this transient. However, this is not crucial as the arm currents do not reach unacceptable levels, slightly exceeding the grid current for a brief period of time. Lastly, the system is still able to control the grid current during the transient while maintaining its sinusoidal shape due to the weighting factors ($\lambda_0 = 1$ & $\lambda_1 = 0.8$) used in the cost function of stage-I of the MPC. Thus, the dual-stage MPC prioritizes following the grid reference currents over minimizing CCs. Finally, as the grid reference current is fed from the voltage loop control mentioned in section 4.1.4, the DC-Link-1 voltage is restored to its reference value, mitigating the disturbance created by the load variation and quickly restoring normal functioning.

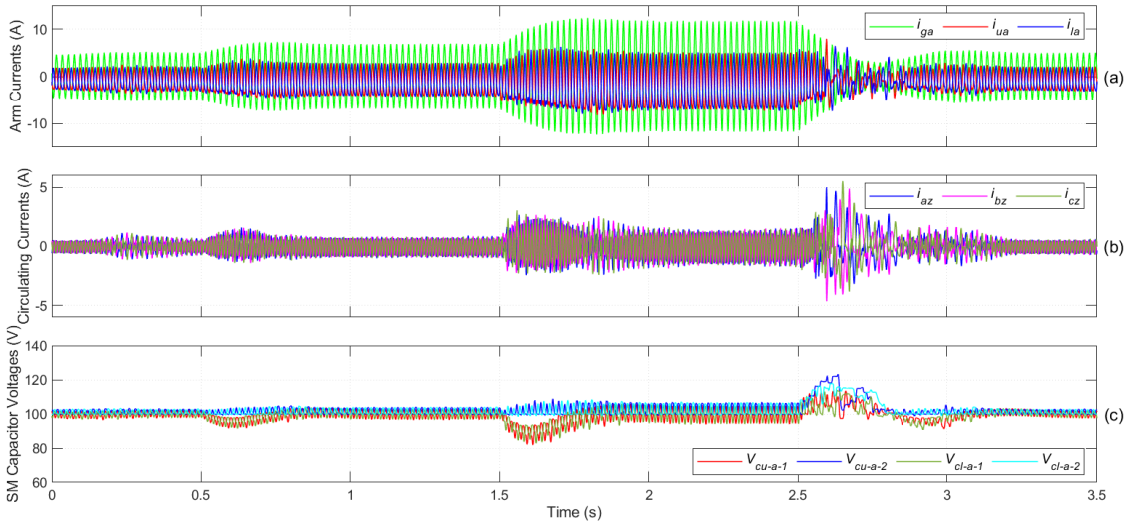


Figure 5.6: MMC dynamic performance: (a) Arm Currents phase-a. (b) Circulating currents all phases. (c) SMs Capacitor voltages, phase-a.

5.1.2.1 Circulating Current Control Turned Off

The same tests were carried out with a zero CC gain ($\lambda_1 = 0$), to demonstrate how CCs affected the system's dynamic performance. In Fig. 5.7, the initial conversion stage variables are shown, and in Fig. 5.8, the MMC's inner variables are seen. The system can cope with load changes, keeping the DC-Link-1 voltage around its reference value, since the cost function (f_0) sole objective is to follow the grid reference current, which is fed via the voltage loop control, as explored in the previous section. Despite this, the DC-link-1 current's ripple has increased, which is explained by the unbalanced nature of the arm currents, which are linked by Eq. 3.2. Furthermore, the arm currents adopt unbalanced waveforms and have their RMS value increased due to the uncontrolled CCs, which clearly show elevated values throughout the test when compared to their respective waveforms in Fig. 5.6 (b). Furthermore, the SMs capacitor voltages ripple have increased when compared to the previous test, as to be expected, due to their relationship with the arm currents as mentioned in the previous section. This test emphasizes the need for CC minimization in achieving balanced and efficient operation of the MMC converter.

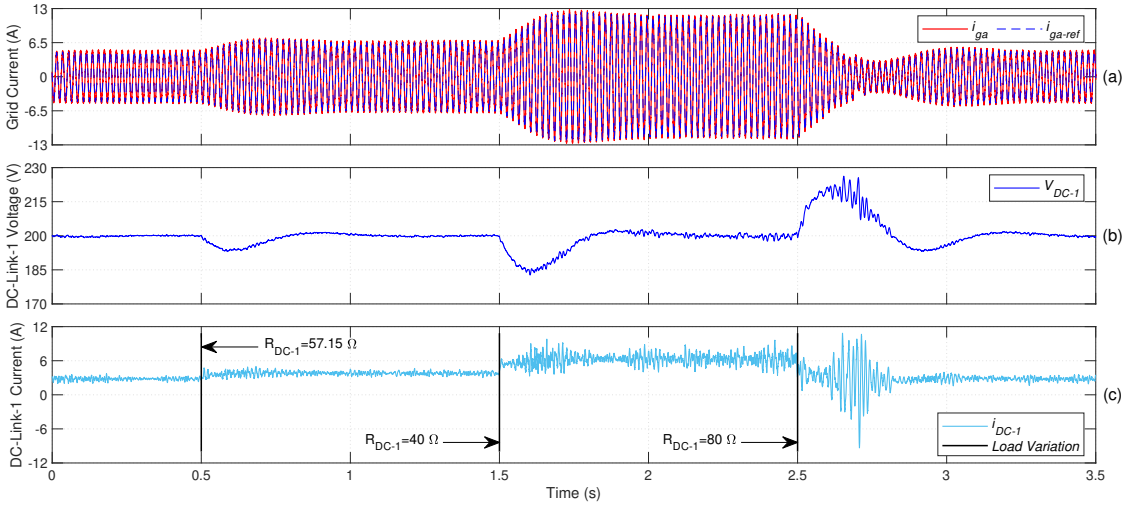


Figure 5.7: First stage dynamic performance (with $\lambda_1 = 0$): (a) Grid currents. (b) DC-Link-1 Voltage. (c) DC-Link-1 Current.

5.1.3 Grid Voltage Disturbance Analysis

A test with four disturbances was forced to the system while it was running at its nominal power, with the goal of testing the robustness of the dual-stage MPC control algorithm against grid voltage disturbances. The waveforms of the first stage during the test are represented in Fig. 5.9. The simulation begins with a standard grid voltage. A 5% voltage drop in the grid voltage of phase a is forced at $t = 0.2$s and lasts for 0.1s. The identical method was applied to phases b and c at $t = 0.4$s and $t = 0.6$s, respectively. Finally, a voltage drop of 5% was imposed on all three phases at $t = 0.9$s. When looking at the waveform of the DC-Link-1 voltage represented in Fig. 5.9 (c), it's clear that there's a slight voltage drop since the system is drawing less power from the grid as a result of the voltage disturbance. However, the voltage loop control described in Fig. 4.3

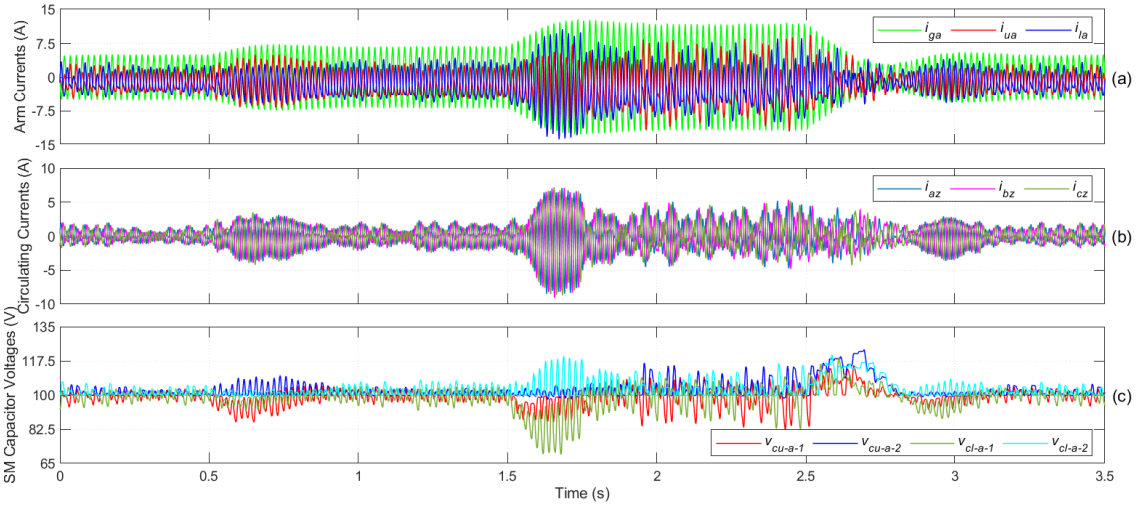


Figure 5.8: MMC dynamic performance (with $\lambda_1 = 0$): (a) Arm Currents, phase-a. (b) Circulating currents. (c) SMs Capacitor voltages, phase-a.

detects this and increases the grid current reference slightly to compensate. The converter is able to ”follow” the reference current during the disturbance, as the measured grid voltages are being directly fed to the MPC algorithm through Eq. 3.7. Thus, the system can preview the grid current behaviour and pick the optimal switching state. As a result, the system can efficiently deal with the three disturbances while maintaining a DC-Link-1 voltage that is near to the reference value, only hitting a drop of 1V. Finally, when the voltage lowers instantly on all three phases during the last disturbance, the DC-Link-1 voltage drop is larger, reaching 2V. The grid reference current is increased by the voltage loop to compensate, as shown in Fig. 5.9 (b). As a result, the higher grid currents compensate for the three-phase voltage loss, and the DC-Link-1 voltage quickly returns to its reference value. After 0.1s, the disturbance stops, and the system returns to its original steady state at nominal power.

5.1.4 MPC Parameter Variation Robustness Analysis

5.1.4.1 Grid Filter Inductance Variation

A number of tests were carried out with the goal of examining the robustness of the MPC algorithm in the presence of parameter fluctuation while the system is running at near its nominal power. Given that inductances used in real-world applications may have a real value higher than rated, the analysis begins by increasing the inductance of the grid filter in phase-a by 1% above the rated value (5mH), which is taken into consideration by the dual-stage MPC model. Table 5.2 shows the variables that were captured during the simulation and are relevant to the analysis. When comparing the values to those in Table 5.1 for steady-state operation with no parameter variations, it is clear that the system can handle the variation as the DC-Link-1 voltage is controlled around its reference value with the same voltage ripple. Furthermore, it is observable that the line-to-line voltage harmonic distortion, $V_{ab-THD}(\%)$, and grid current harmonic distortion, $I_{g-THD}(\%)$, maintain a value that is nearly equivalent to the steady-state operation. Given that inductance

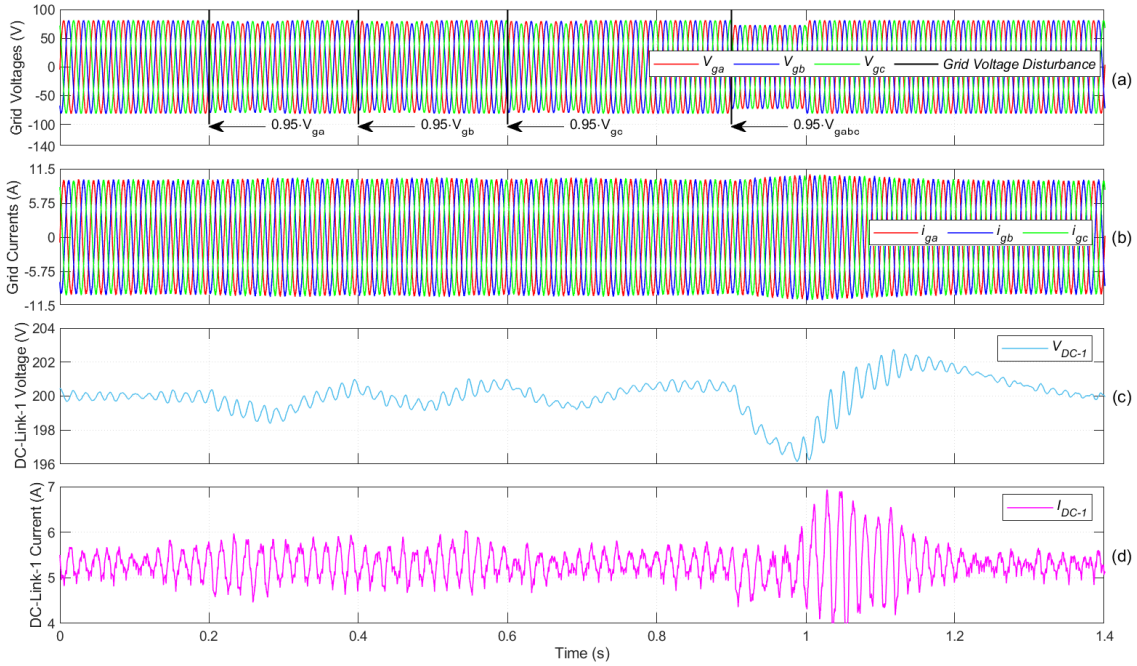


Figure 5.9: First stage performance under grid voltage disturbances: (a) Grid Voltages. (b) Grid Currents. (c) DC-Link-1 Voltage. (d) DC-Link-1 Current.

values tend to decrease with ageing in real life, it makes sense to test the MPC with grid filter values lower than the rated value. Thus, the value of the grid filter inductance of phase-a, L_{fa}, was varied until 70% in steps of 10% to record the performance variables of the first stage. Both $V_{ab-THD}(\%)$ and $I_{g-THD}(\%)$ are expected to rise when the steps are taken. However, these do not reach inadmissible quantities, even in the worst analyzed situation of $L_{fa} = 0.7 \cdot L_{f-nom}$.

Table 5.2: First stage performance values with grid filter inductance variations in phase a.

$\frac{L_{fa}}{L_{f-nom}}$	$V_{DC-1-Ripple}(V)$	$i_{DC-1-Ripple}(A)$	$V_{ab-THD}(\%)$	$I_{g-THD}(\%)$
1.1	0.5	0.7	31.64	2.12
0.9	0.5	0.5	30.96	2.31
0.8	0.4	0.5	30.8	2.44
0.7	0.5	0.7	30.21	2.53

The procedure was repeated, but this time the inductances in all three phases were varied simultaneously. The acquired results are listed in Table 5.3. As previously, for the first test, a value higher than the rated value by 10% is used in all three phases. The system responds well to such changes since the DC-Link-1 voltage is kept close to its reference value, and the voltage and current harmonic distortion are similar to those shown in Table 5.1 for the steady-state study. The harmonic values tend to degrade as the variation increases, as one might predict. Despite this, the system is still able to control the voltage on DC-Link-1. For the worst-case scenario of $L_{f-abc} = 0.7 \cdot L_{f-nom}$, the system still presents good performance values. Finally, it is possible to conclude that the dual-stage MPC algorithm is extremely robust to grid filter parameter fluctuation.

Table 5.3: First stage performance values with grid filter inductance variations in all phases.

$\frac{L_{f-abc}}{L_{f-nom}}$	$V_{DC-1-Ripple}(V)$	$i_{DC-1-Ripple}(A)$	$V_{ab-THD}(\%)$	$I_{g-THD}(\%)$
1.1	0.6	0.7	31.79	2.12
0.9	0.4	0.7	30.7	2.35
0.8	0.4	0.5	30.58	2.54
0.7	0.3	0.6	30.59	2.75

5.1.4.2 MMC Arm Inductance Variation

This section, like the previous one, aims to investigate the dual-stage MPC robustness to parameter variation, but this time in the scope of MMC arm inductance, L_m, variation. Two sets of testing were carried out. The performance values for the first one, which is related to the variation of both the upper and lower arm inductance in phase-a, are shown in Table 5.4. Table 5.5 shows the results of the second series of tests, which are focused on the variation of the arm's inductances in all phases (L_{m-abc}).

Initially, examining the system's performance with solely variations in phase a's arm inductances, L_{m-au} & L_{m-al}, the system can cope with the fluctuation, maintaining the DC-Link-1 voltage regulated around its reference value, and the harmonic distortion values maintain a correct value. The average value of arm currents in the three phases tends to grow in the subsequent tests of decreasing L_{m-a} in steps of 10% until $L_{m-a} = 0.7 \cdot L_{m-nom}$. This is to be expected since the arm's impedance value is lowered. Nonetheless, until the very last variation, the system appears to respond adequately. The last L_{m-a} value destabilizes the system because the DC-Link-1 current has a large current ripple of 1.8A, which is explained by the DC-Link-1 current model in Eq. 3.1 and Eq. 3.2. Despite this, the system can endure a wide range of fluctuations in one phase's leg inductances.

Table 5.4: First stage performance values with MMC arm inductance variations in phase a.

$\frac{L_{m-a}}{L_{m-nom}}$	$V_{DC-1-Ripple}(V)$	$i_{DC-1-Ripple}(A)$	$V_{ab-THD}(\%)$	$I_{g-THD}(\%)$	$AVG\ I_{grid-RMS}(A)$	$AVG\ I_{arms-RMS}(A)$	$AVG\ I_{circ-RMS}(A)$
1.1	0.4	0.5	30.86	2.18	6.62	3.83	0.77
0.9	0.6	0.7	31.74	2.29	6.6	3.84	0.84
0.8	0.6	0.9	32.56	2.34	6.6	3.84	0.89
0.7	1.8	1.8	32.90	2.38	6.59	3.89	0.99

Finally, when testing the systems against variations in L_m in all 6 filters (2 arms & 3 legs), it is evident that the system can cope and maintain good performance, with a controlled DC-Link-1 voltage and low THD values, for the first variation of a 10% increment. However, as the variation decreases, the average CC in all three phases dramatically increases, which makes sense because the arms' impedance drops, and the average RMS arm current value rises, resulting in reduced converter efficiency. The average RMS grid current value remains constant because the converter can still control the grid currents correctly with a low THD value. The average RMS grid current value remains constant because the converter can still control the grid currents correctly with a low THD value. Notably, changing the MMC's arm inductances has a stronger impact on its inner variables, with increased CCs affecting the DC-Link-1 current, as described in the preceding

paragraph, resulting in a larger DC-Link-1 voltage and current ripple. To summarize, the MPC dual-stage algorithm is very robust to parameter variation, as it can effectively control grid currents. The discretization model used in Eq. 3.7 combined with the MPC controller's low sampling time, as the real grid currents are fed to the controller, the controller can keep track and predict grid current behaviour. Thus, the system is able to compensate for parameter deviation error, picking the optimal switching state. However, this inaccuracy can only be compensated up to a certain point, as the first stage conversion performance degrades when the deviation increases.

Table 5.5: First stage performance values with MMC arm inductance variations in all phases.

$\frac{L_{m-abc}}{L_{m-nom}}$	$V_{DC-1-Ripple}(V)$	$i_{DC-1-Ripple}(A)$	$V_{ab-THD}(\%)$	$I_{g-THD}(\%)$	$AVG\ I_{grid-RMS}(A)$	$AVG\ I_{arms-RMS}(A)$	$AVG\ I_{circ-RMS}(A)$
1.1	0.3	0.35	30.12	2.16	6.62	3.82	0.7
0.9	1.4	1.5	32.09	2.37	6.6	3.93	1.23
0.8	1.7	2.3	33.35	2.45	6.58	4.07	1.55
0.7	2.4	3	34.66	2.67	6.59	4.17	2.14

5.2 Second Conversion Stage

5.2.1 Steady-State Performance Analysis

To test the performance of the second conversion stage, a 9Ω DC load was introduced into the DC-Link-2. The waveforms derived from the simulation are shown in Fig. 5.10. The findings are consistent with the analyses presented in section 4.2, Fig. 4.4. The winding Voltages of the HFT are shown in Fig. 5.10 (a). Two square waves with a switching frequency of $f_d = 5$kHz are displayed, as expected, with a phase shift difference provided by the voltage loop control described in subsection 4.2.2. The voltage reaches a peak-to-peak value of 200V on the DC-Link-1 side (primary side, V_{AC-1}), and a peak-to-peak value of 100V on the DC-Link-2 side (secondary side, V_{AC-2}). Because the second conversion stage is working in buck mode, delivering power from the DC-Link-1 to the DC-Link-2, V_{AC-1} is in advance in relation to V_{AC-2}. Furthermore, the input current of the second stage has a lower RMS value than the output current, which is to be expected, given that the input and output powers are roughly equal. Because of the ISOP architecture, the output current is divided between the two DAB converters used for the second stage. Finally, looking at the DC-Link-2 voltage in Fig. 5.10. (c), it is clear that the second conversion stage is capable of controlling the voltage since its value only reaches a ripple of 1.5V around its reference value of 90V.

5.2.2 Dynamic Performance Analysis

With the purpose of testing the dynamic performance of the first conversion stage, load variations on the DC-Link-2 were imposed. The simulation begins with a DC-Link-2 load (R_{DC-2}) of 12Ω. The load is increased to 9Ω at $t = 0.5$s. As a result, the DC-Link-2 voltage, as shown in Fig. 5.11 (b), drops around 9V. However, as described in subsection 4.2.2, the PI controller quickly responds and regulates the phase-shift (φ) as represented in Fig. 5.11 (c). Consequently, the voltage is regulated back to its reference value of 90V. The same procedure is repeated at $t =$ 1s with $R_{DC-2} = 18\Omega$, $t =$1.5s with $R_{DC-2} =$36 Ω, and finally, at $t = 2$s, R_{DC-2} is restored to

it's original value. In all variations, it is statable that the response time is not very quick. However this is not crucial, since the main control objective is to keep the DC-Link-2 voltage around its reference value, avoiding voltage variations over 10%, maintaining the PQ on the DC-Link-2.

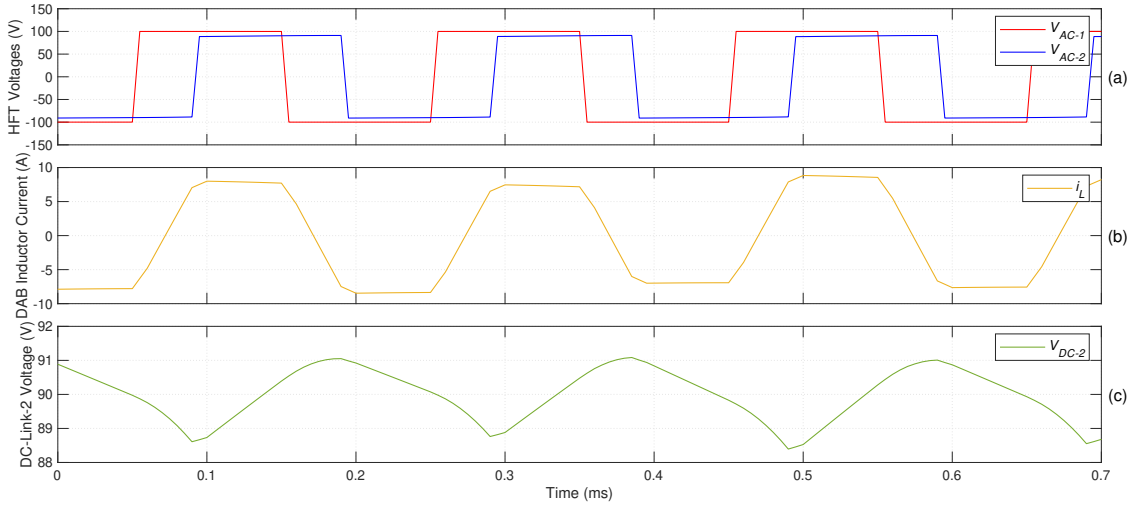


Figure 5.10: Second stage steady-state performance: (a) HFT's Winding Voltages. (b) DAB Inductor Current. (c) DC-Link-2 Voltage.

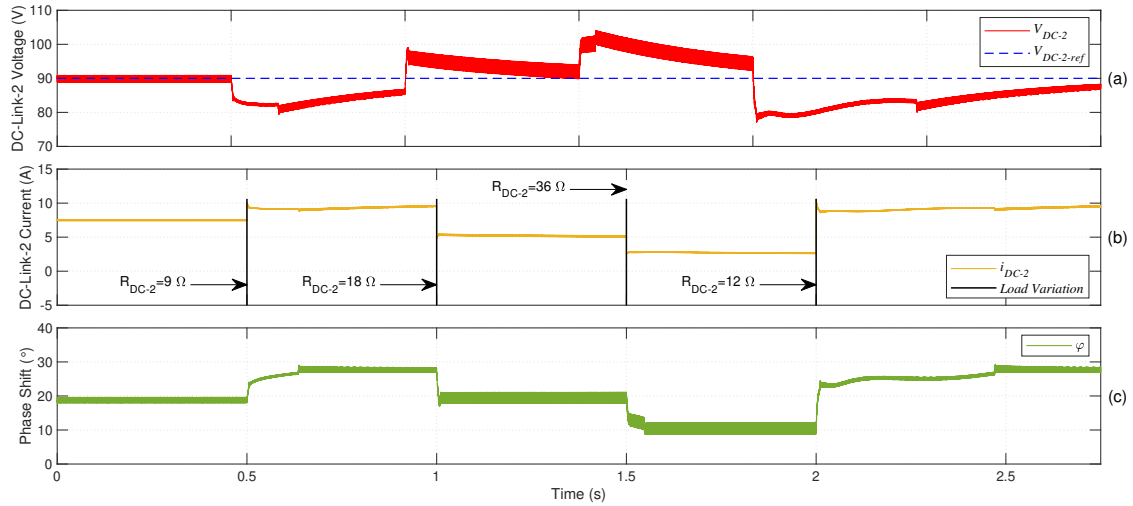


Figure 5.11: Second stage dynamic performance: (a) DC-Link-2 Voltage. (b) DC-Link-2 Current. (c) DAB's phase shift.

5.3 Battery Storage System

5.3.1 Control Analysis

5.3.1.1 Battery Charging

The following tests were conducted to demonstrate the control capabilities of the BSS for different charging rates of the battery pack. Since the SST main focus is to enable power flow from the BSS to the electrical grid and viceversa, in periods of low demand, it could be desirable to flood out some of the excess energy out of the grid, thus it makes sense that the system can charge the BSS with different charging rates in order to maintain the grid balance. Nevertheless, the different charging regimes should not impact the overall system's performance. Therefore, a simulation test was conducted to test the system at different charging regimes. The respective results are displayed in Fig. 5.12. The simulation starts with $R_{DC-2} = 17\Omega$. At $t = 0.5$s, the battery pack is connected to the DC-Link-2 and R_{DC-2} is disconnected. Thereafter, the pack is charged at different rates. It is notable that the SST is able to charge the BSS with different charging currents (I_{BAT}) as represented in Fig. 5.12 (c), without jeopardizing the overall voltage stability of the SST as portrayed in Fig. 5.12(a) & (b). As to be expected the battery's pack State of Charge (SOC) also increases with different rates as represented in Fig. 5.12 (d), validating the functioning of the DC-DC converter.

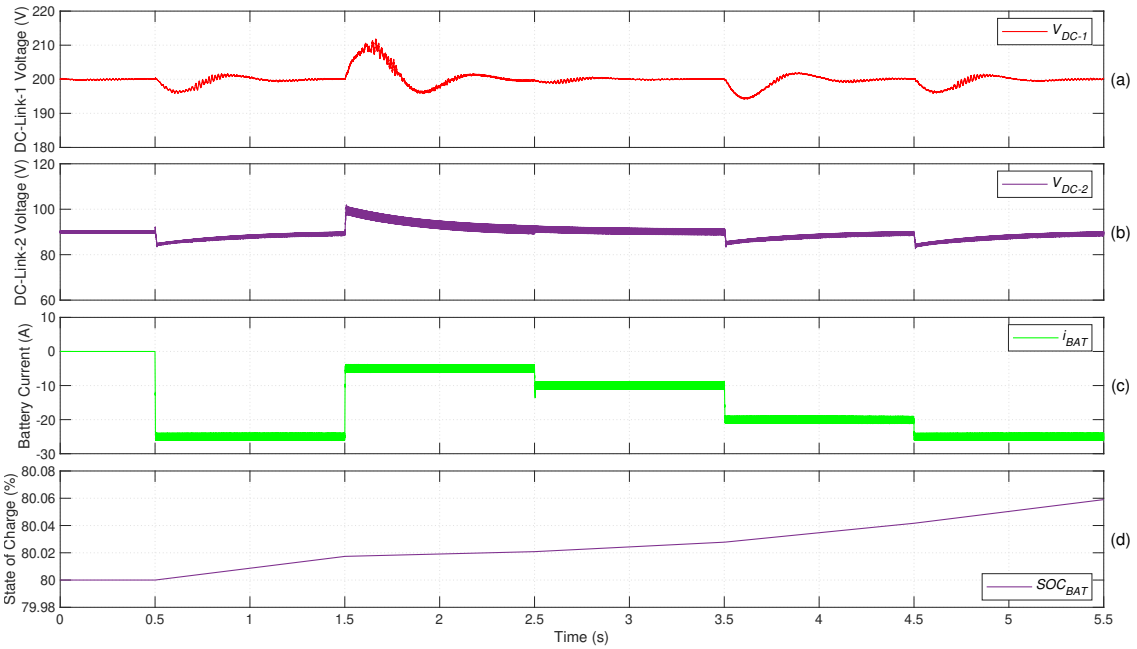


Figure 5.12: BSS charging at different rates:(a) DC-link-1 Voltage. (b) DC-link-2 Voltage. (c) Battery Pack Current. (d) Battery Pack SOC.

5.3.1.2 Battery Discharging

Making a similar analysis to the previous subsection, the following tests were conducted to demonstrate the control capabilities of the BSS for discharging the battery pack at different rates, as it could be desirable to feed more or less power to the grid depending on the load demand. Nevertheless, the different discharging rates should not impact the overall system's performance. In that sense, a simulation test was conducted, testing the system's performance at different discharging rates, the respective results are displayed in Fig. 5.13. The simulation starts with a battery current of 15A. At $t = 1$s the battery pack's current reference is set to 22.5A. Thereafter, different discharge current rates are applied. It is notable that the BSS is discharging at different rates as represented in Fig. 5.13 (a), without jeopardizing the overall voltage stability of the SST as portrayed in Fig. 5.13 (a) & (b). As to be expected the battery's pack SOC decreases with different rates as represented in Fig. 5.13 (d).

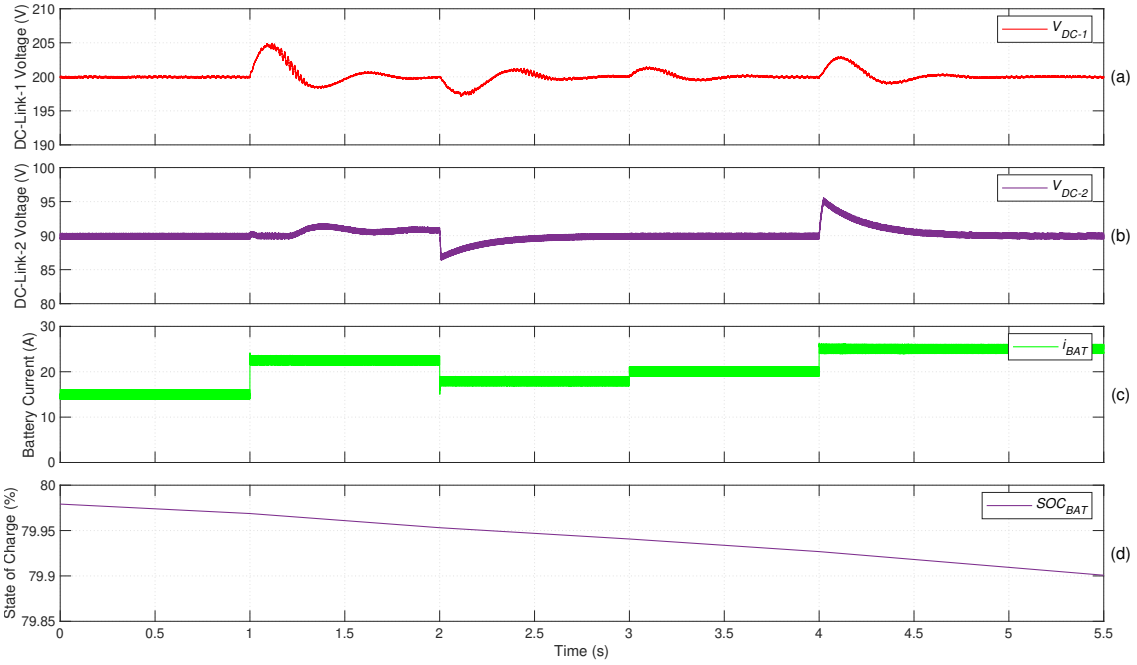


Figure 5.13: BSS discharging at different rates:(a) DC-link-1 Voltage. (b) DC-link-2 Voltage. (c) Battery Pack Current. (d) Battery Pack SOC.

5.4 Power-flow Analysis

The purpose of the following sector is to prove the well functioning of the SST by analysing the power flow of the system under load variations and battery charge and discharge regimes. In Fig.5.14 the system's power-flow is depicted. A 2 second interval is used to introduce changes to the system, which include charging and discharging the BSS and adding loads to the DC-Links. At t =0s there is no load demand and the BSS and second stage are disconnected.

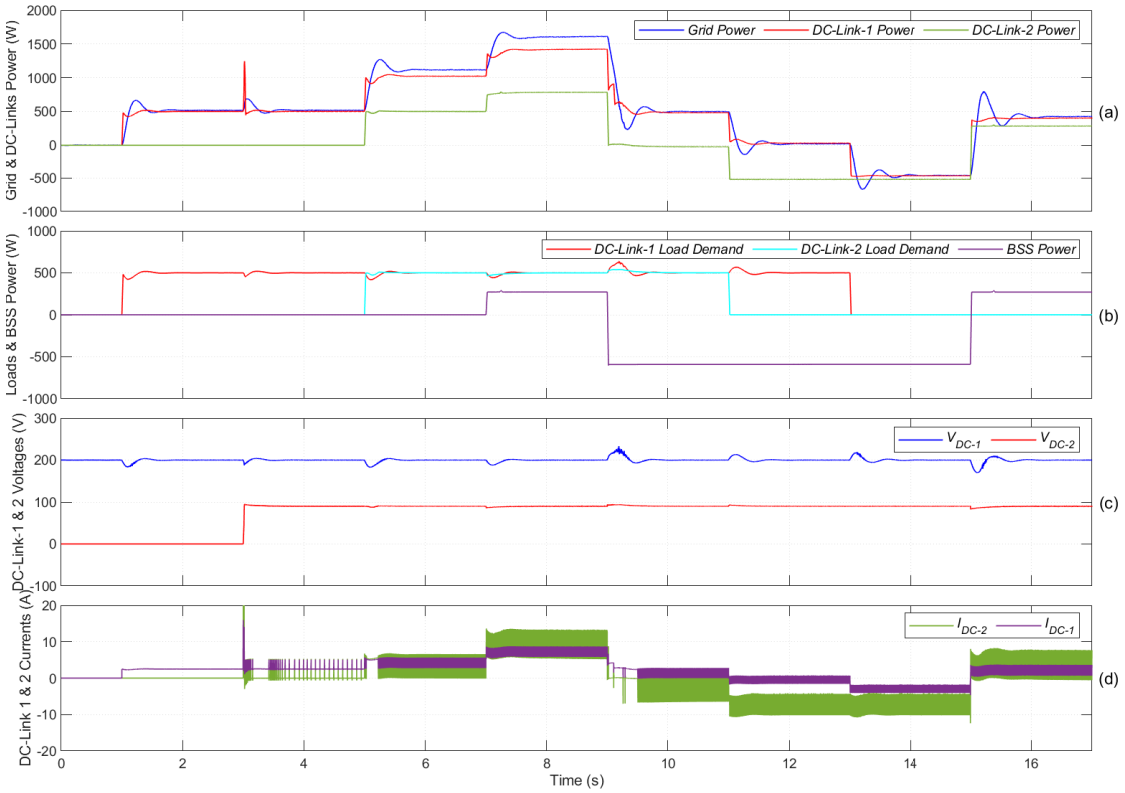


Figure 5.14: Power-flow analysis: (a) Grid Power. (b) Battery Pack Power. (c) DC-Link 1 & 2 Voltages. (d) DC-Link 1 & 2 Currents.

A load of 500W is added in DC-Link 1 at t = 1s resulting in a grid power increase. The DC-Link 2 is only connected at t =3 s in order to start the system sequentially; though this generates a transient, it has no impact on the grid's power demand as there is no load on the DC-Link 2. A load of 500W is added into DC-Link 2 at t =5s, increasing the power grid to 1000W. The grid power demand also increases at t =7s when the BSS is connected and charged at a rate of 300W. At t =9s, the BSS starts providing power to the system. As a result, the grid's power need is of 500W as both loads are still connected. The load on DC-Link-2 is disconnected at t = 11s, causing the system to stop consuming power from the grid and the load on DC-Link-1 is disconnected at t = 13s. Since there are no additional loads in the system, the power supplied from the battery is totally fed to the grid. At t = 15s, the battery restarts power consumption and receives a 300W charge. The voltage and currents in the system are well distributed as depicted in Fig. 5.14 (d) proving that the system can adjust and distribute power properly despite the introduced load variations.

Chapter 6

Conclusion and Future Work

6.1 Conclusions

This dissertation proposed a Solid-State Transformer application for integrating an energy storage system. The foregoing discussion has begun with a brief state-of-the-art of how SST technology was developed, which included the various SST architectures that are dependent on the number of conversion stages used. Furthermore, the various types of converters used are succinctly examined, as well as the SST's key component, the HFT. To conclude chapter 1, the major SST's applications are presented, to give a more thoughtful insight of the applicability of the technology in nowadays world.

With regard to the two-stage conversion SST design with an HVDC-Link incorporated in the battery pack into the HVAC electrical grid, the Modular Multilevel Converter (MMC) was chosen for the first conversion stage (HVAC-HVDC) as it meets the HV criteria due to its scalability and modularity. For the second conversion stage, because of their simple control and configuration, galvanic isolation and bidirectional capabilities, the Dual-Active Bridge (DAB) converters were chosen in an ISOP connection. Finally, a BSS is elected, which consists in a lithium-ion battery pack and a DC-DC converter for charging and discharging the battery pack correctly.

To continue the investigation, the system's mathematical model was then given by starting the first conversion stage, presenting the discrete-time model of the MMC in a three-phase approach due to its improved performance and the grid connection. The SM discrete-time model is also described besides the modeling of the DAB converter, which is used in the second conversion stage. Following the presentation of the mathematical model of the system, the control of the system is then investigated. In comparison to the converter's typical control techniques (PI & PWM), the MPC approach was chosen for the MMC because it has a higher dynamic response and controlability. For the second conversion stage, the simple SPS control method was selected.

A simulation analysis was conducted using MATLAB/Simulink to validate the performance of the proposed system and its associated control techniques. The steady-state and dynamic performances of the MMC, employed in the first conversion stage, are studied under different load

demands, grid voltage disturbances and parameter variation in a detailed analysis. Different load regimes are used to assess the second conversion stage performance. At last, the BSS is put to the test for various charging and discharging regimes.

The intention of this dissertation is to enhance the academic understanding of SST technology, with a main focus of developing a control algorithm for the MMC converter. The simulation results have proven that the MMC performs competently/effectively in both steady-state and dynamic operation using the designed control system, with all of the converter's control objectives met. The converter also performed well during grid voltage disturbances and was extremely resistant to parameter variations. The second conversion stage also displayed a good steady-state and dynamic performance, however its efficiency could be improved through further development of its control system.

To sum up, the BSS was charged and discharged at different rates, thus consuming and providing energy to electrical grid while maintaining a good overall system's performance, proving the system's bidirectional capabilities and validating the successful implementation of the SST application.

6.2 Suggestions for Future Work

Suggestions for further research can be made based on the developed work and results reported in this dissertation:

- Implement the proposed SST application in a real environment;
- Develop an MPC algorithm for the MMC converter which directly predicts and controls the arms currents as presented in [35], to further improve the converter's efficiency and performance;
- Further develop the control strategies employed in the second conversion stage to help improve the system's overall efficiency even more;
- Develop a BSS algorithm to correctly charge & discharge the battery pack in accordance to its requirements.

Bibliography

[1] IEA-ETSAP and IRENA (2015), Renewable Energy Integration in Power Grids: Technology Brief. page 36.

[2] Ahmed Abu-Siada, Jad Budiri, and Ahmed Abdou. Solid State Transformers Topologies, Controllers, and Applications: State-of-the-Art Literature Review. *Electronics*, 7(11):298, November 2018.

[3] K.H. Ahmed, S.J. Finney, and B.W. Williams. Passive Filter Design for Three-Phase Inverter Interfacing in Distributed Generation. In *2007 Compatibility in Power Electronics*, pages 1–9, Gdansk, Poland, May 2007. IEEE.

[4] Mark S. Allen. Innovation for Life. *The Annals of Thoracic Surgery*, 102(5):1417–1425, November 2016.

[5] Nuno Martins Alves. High-Performance Isolated Bidirectional DC-DC Converter. page 140.

[6] Apparao Dekka, Bin Wu, Venkata Yaramasu, Ricardo Lizana Fuentes, and Navid R. Zargari. Model Predictive Control of High-Power Modular Multilevel Converters—An Overview. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 7(1):168–183, March 2019.

[7] Apparao Dekka, Bin Wu, Venkata Yaramasu, and Navid R. Zargari. Dual-Stage Model Predictive Control With Improved Harmonic Performance for Modular Multilevel Converter. *IEEE Transactions on Industrial Electronics*, 63(10):6010–6019, October 2016.

[8] Apparao Dekka, Bin Wu, Venkata Yaramasu, and Navid R. Zargari. Integrated model predictive control with reduced switching frequency for modular multilevel converters. *IET Electric Power Applications*, 11(5):857–863, May 2017.

[9] Apparao Dekka, Bin Wu, Venkata Yaramasu, and Navid Reza Zargari. Model Predictive Control With Common-Mode Voltage Injection for Modular Multilevel Converter. *IEEE Transactions on Power Electronics*, 32(3):1767–1778, March 2017.

[10] Apparao Dekka, Bin Wu, and Navid R. Zargari. Minimization of DC-Bus Current Ripple in Modular Multilevel Converter Under Unbalanced Conditions. *IEEE Transactions on Power Electronics*, 32(6):4125–4131, June 2017.

[11] Sixing Du, Apparao Dekka, B. Wu, and Navid Zargari. *Modular multilevel converters: analysis, control, and applications*. Number 67 in IEEE Press series on power engineering. IEEE Press ; Wiley, Piscataway, NJ : Hoboken, New Jersey, 2018.

[12] Herbert Bristol Dwight. Skin effect and proximity effect in tubular conductors. *Journal of the American Institute of Electrical Engineers*, 41(3):203–209, March 1922.

[13] M. Ebrahim Adabi, Juan A. Martinez-Velasco, and Universitat Politecnica de Catalunya, Barcelona, Spain. Solid state transformer technologies and applications: A bibliographical survey. *AIMS Energy*, 6(2):291–338, 2018.

[14] Christian Fontana. *Solid State Transformer*. PhD thesis, UNIVERSITÀ DEGLI STUDI DI PADOVA, 2018.

[15] Kenny George. Design and Control of a Bidirectional Dual Active Bridge DC-DC Converter to Interface Solar, Battery Storage, and Grid-Tied Inverters. page 95.

[16] Sarah Saeed Hazkial Gerges. Ph.D. THESIS DISSERTATION. page 310.

[17] M.A. Hannan, M.S.H. Lipu, A. Hussain, and A. Mohamed. A review of lithium-ion battery state of charge estimation and management system in electric vehicle applications: Challenges and recommendations. *Renewable and Sustainable Energy Reviews*, 78:834–854, October 2017.

[18] Mahammad A. Hannan, Pin Jern Ker, Molla S. Hossain Lipu, Zhen Hang Choi, M. Safwan Abd. Rahman, Kashem M. Muttaqi, and Frede Blaabjerg. State of the Art of Solid-State Transformers: Advanced Topologies, Implementation Issues, Recent Progress and Improvements. *IEEE Access*, 8:19113–19132, 2020.

[19] PEREIRA Ivo. Multicarrier and Space Vector Modulation for Three-Phase NPC Converters: A Comparative Analysis. page 11, 2009.

[20] Jiangchao Qin and M. Saeedifard. Predictive Control of a Modular Multilevel Converter for a Back-to-Back HVDC System. *IEEE Transactions on Power Delivery*, 27(3):1538–1547, July 2012.

[21] Jaehong Kim, Hong-Seok Song, and Kwanghee Nam. Asymmetric Duty Control of a Dual-Half-Bridge DC/DC Converter for Single-Phase Distributed Generators. *IEEE Transactions on Power Electronics*, 26(3):973–982, March 2011.

[22] Mahbubur Rahman Kiran, Omar Farrok, Md. Rabiul Islam, and Jianguo Zhu. Characterization of the Optimized High Frequency Transformer Using Nanocrystalline and Amorphous Magnetic Materials. In *2019 22nd International Conference on Electrical Machines and Systems (ICEMS)*, pages 1–4, Harbin, China, August 2019. IEEE.

[23] Marco Liserre, Giampaolo Buticchi, Markus Andresen, Giovanni De Carne, Levy Ferreira Costa, and Zhi-Xiang Zou. The Smart Transformer: Impact on the Electric Grid and Technology Challenges. *IEEE Industrial Electronics Magazine*, 10(2):46–58, June 2016.

[24] Haining Liu, Ijaz Haider Naqvi, Fajia Li, Chengliang Liu, Neda Shafiei, Yulong Li, and Michael Pecht. An analytical model for the CC-CV charge of Li-ion batteries with application to degradation analysis. *Journal of Energy Storage*, 29:101342, June 2020.

[25] Roberto Panchev, Hristian Panchev, Vladimir Chikov, and Rumen Kirov. Study on Influence of Current and Voltage Harmonics on the Reliability and Life Expectancy of Power Transformers. In *2019 11th Electrical Engineering Faculty Conference (BulEF)*, pages 1–4, Varna, Bulgaria, September 2019. IEEE.

[26] Rafael Pena-Alzola, Ghanshyamsinh Gohil, Laszlo Mathe, Marco Liserre, and Frede Blaabjerg. Review of modular power converters solutions for smart transformer in distribution system. In *2013 IEEE Energy Conversion Congress and Exposition*, pages 380–387, Denver, CO, USA, September 2013. IEEE.

[27] Delmiro João Rego Pereira. Transformador Eletrónico de Potência como Solução para a Regulação da Tensão e Frequência em Redes Elétricas Isoladas. page 103.

[28] Dionisio Ramirez, Mohammad Ebrahim Zarei, Mahima Gupta, and Javier Serrano. Fast Model-based Predictive Control (FMPC) for grid connected Modular Multilevel Converters (MMC). *International Journal of Electrical Power & Energy Systems*, 119:105951, July 2020.

[29] D. Rathod. Solid State Transformer (SST) - "Review of Recent Developments", Advance in Electronic and Electric Engineering, Research India Publications. page 6.

[30] Yann G. Rebours, Daniel S. Kirschen, Marc Trotignon, and Sbastien Rossignol. A Survey of Frequency and Voltage Control Ancillary Services—Part I: Technical Features. *IEEE Transactions on Power Systems*, 22(1):350–357, February 2007.

[31] Dr. Ashok S. Solid State Transformers, National Institute of Technology (NIT), Calicut. page 137.

[32] Deshang Sha and Guo Xu. *High-Frequency Isolated Bidirectional Dual Active Bridge DC–DC Converters with Wide Voltage Gain*. CPSS Power Electronics Series. Springer Singapore, Singapore, 2019.

[33] Mohammed Azharuddin Shamshuddin, Felix Rojas, Roberto Cardenas, Javier Pereda, Matias Diaz, and Ralph Kennel. Solid State Transformers: Concepts, Classification, and Control. *Energies*, 13(9):2319, May 2020.

[34] Aniel Shri. *A Solid-State Transformer for Interconnection Between the Medium- and the Low-Voltage Grid*. PhD thesis, Delft University of Technology, October 2013.

[35] Zhen Wang, Xianggen Yin, and Yu Chen. Model Predictive Arm Current Control for Modular Multilevel Converter. *IEEE Access*, 9:54700–54709, 2021.

[36] Xu She, Alex Q. Huang, and Rolando Burgos. Review of Solid-State Transformer Technologies and Their Application in Power Distribution Systems. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 1(3):186–198, September 2013.

[37] V. Yaramasu, J. Rodriguez, B. Wu, M. Rivera, A. Wilson, and C. Rojas. A simple and effective solution for superior performance in two-level four-leg voltage source inverters: Predictive voltage control. In *2010 IEEE International Symposium on Industrial Electronics*, pages 3127–3132, Bari, Italy, July 2010. IEEE.

[38] Jiepin Zhang, Jianqiang Liu, Jingxi Yang, Nan Zhao, Yang Wang, and Trillion Q. Zheng. A Modified DC Power Electronic Transformer Based on Series Connection of Full-Bridge Converters. *IEEE Transactions on Power Electronics*, 34(3):2119–2133, March 2019.

Appendixes

7.1 Overall SST Simulation Model

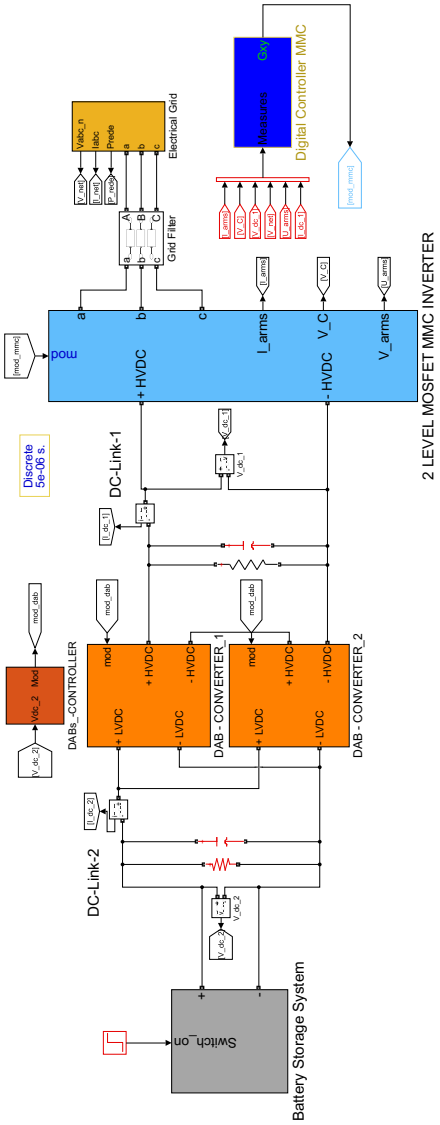


Figure 7.1: SST simulation model.

7.2 MMC & HB-SM Simulation Model

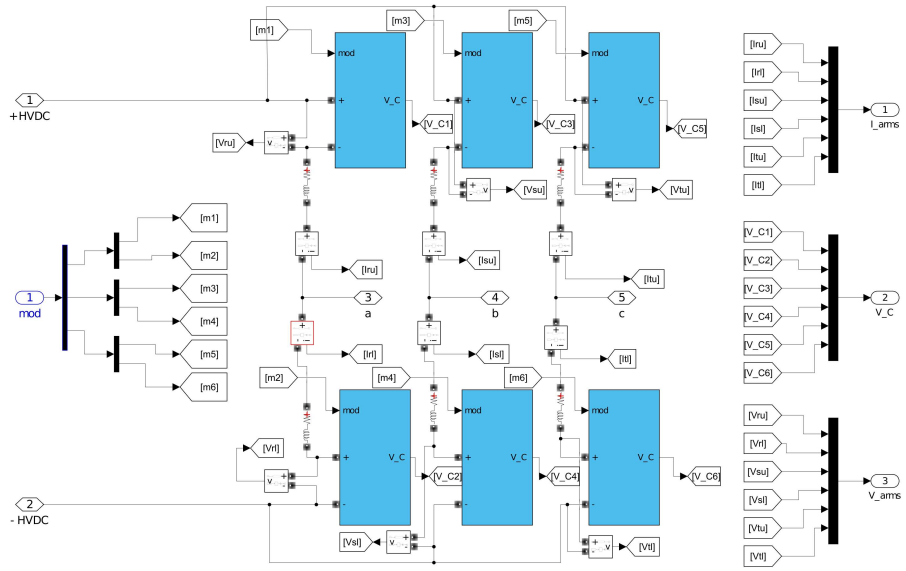


Figure 7.2: MMC simulation model.

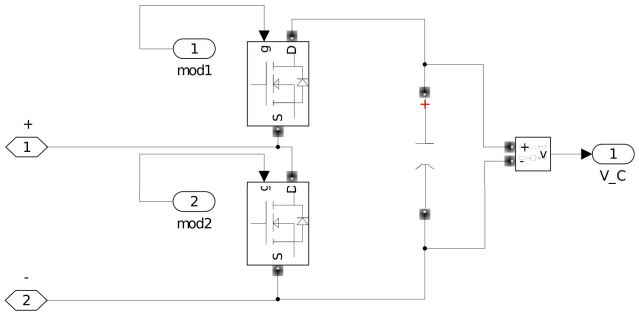


Figure 7.3: HB-SM simulation model.

7.3 DAB Simulation Model

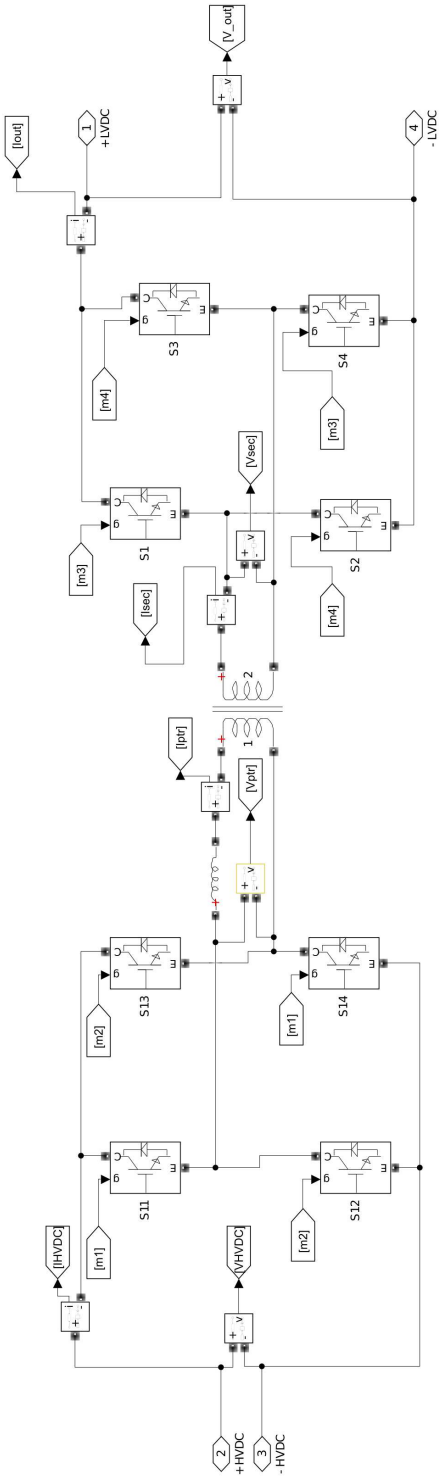


Figure 7.4: DAB simulation model.

7.4 BSS Simulation Model

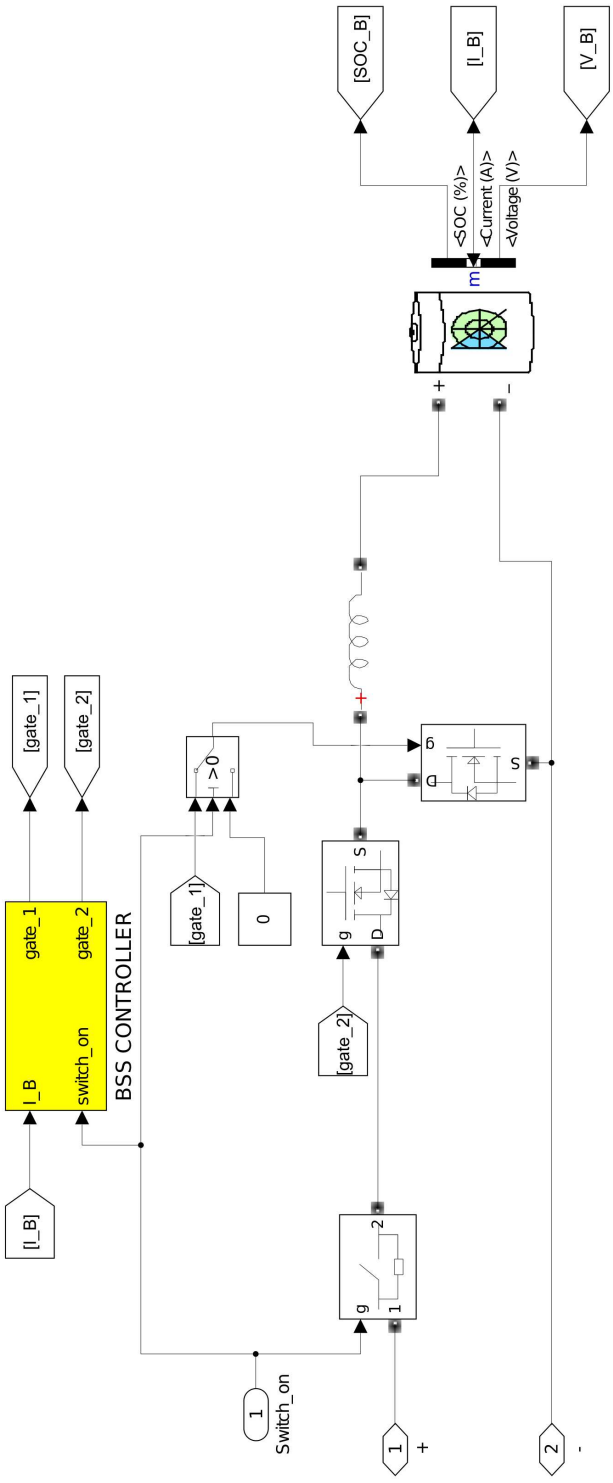


Figure 7.5: BSS simulation model.

7.5 System Parameters used in the Simulation Model

Table 7.1: System parameters.

Variable	Description	Simulation SI
First Conversion Stage		
S_0	Apparent power (KVA)	1
v_{ll}	Grid L-L RMS voltage (V)	100
I_g	Grid RMS current (A)	5.8
f_s	Grid frequency (Hz)	50
L_g	Grid inductance (mH)	0.1
r_g	Grid resistance (Ω)	0.1
L_f	Grid filter inductance (mH)	5
r_f	Grid filter resistance (Ω)	0.2
V_{DC-1}	DC-link-1 voltage (V)	200
C_{DC-1}	DC-link-1 capacitance (mF)	3
N	No. of SMs per arm	2
C_{SM}	SM capacitance (uF)	1880
V_{C-SM}	SM capacitor Voltage (V)	100
L_m	Arm inductance (mH)	4
R_m	Arm inductance resistance (Ω)	0.4
Second Conversion Stage		
V_{DC-2}	DC-link-2 voltage (V)	90
C_{DC-2}	DC-link-2 capacitance (mF)	2.5
N_{DAB}	No. of DAB's coupled in ISOP	2
f_d	DAB switching frequency (kHz)	5
V_1	DAB primary side voltage (V)	100
V_2	DAB secondary side voltage (V)	90
L_1	Primary winding inductance (μ H)	1.07
R_1	Primary winding resistance (Ω)	0.1
L_2	Secondary Winding Inductance (μ H)	1.07
R_2	Secondary Winding Resistance (Ω)	0.1
L_{mag}	Magnetizing inductance (H)	0.15
R_{mag}	Magnetizing resistance (Ω)	1,00E+06
Battery Storage System		
V_{BAT}	Nominal voltage (V)	20
C_{BAT}	Rated capacity (Ah)	40
C_{rate}	Nominal discharge current (A)	17.4

7.6 MPC Stage-I Algorithm Implementation

In the following pages the MPC Stage-I algorithm implementation in a MATLAB/Simulink environment is displayed.

```
function [opt_vector, Irst, Irst_p_opt, Irst_z, Irst_z_p_opt,
 U_arms_p, V_no] = MPC_Stage_1( V_C, V_net, I_arms, Irst_ref, Tsc,
 R_mmc, L_mmc, R_s, L_s)

    %----Constants----%

    Sxy = [0 0 0; 1 1 1; 2 2 2; 1 0 0; 1 1 0; 0 1 0; 0 1 1; 0 0 1; 1 0
 1; 2 1 1; 2 2 1; 1 2 1; 1 2 2; 1 1 2; 2 1 2; 2 0 0; 2 1 0; 2 2 0; 1 2
 0; 0 2 0; 0 2 1; 0 2 2; 0 1 2; 0 0 2; 1 0 2; 2 0 2; 2 0 1];
    N=2;

    fi_o = 1 - (((R_mmc + 2*R_s)*Tsc)/(L_mmc+2*L_s));
    psi_o = Tsc/(L_mmc + 2 * L_s);

    fi_z = 1 - ((6*R_mmc*Tsc)/(6*L_mmc));
    psi_z = Tsc/(6*L_mmc);

    %----Gains----%

    [y_o, y_z]=deal(1,0.8); %Weighting factors used in cost function

    %----References----%

    Irst_z_ref=0;  %Reference for circulating currents

    %----Variables Initialization----%
    ini
    aux_cost=inf;
    j_opt=1;

    Irst_p = [0;0;0];
    Irst_z_p = [0;0;0];

    Irst_p_opt = [0;0;0];
    Irst_z_p_opt = [0;0;0];

    U_arms_p=[0;0;0;0;0;0];

    V_no=0;

    %Measurement and Synthesis of Feedback Signals%

    %Demux

    Iru=I_arms(1);
    Irl=I_arms(2);
    Isu=I_arms(3);
    Isl=I_arms(4);
    Itu=I_arms(5);
    Itl=I_arms(6);
```

```
    Ir=Iru-Irl;
    Is=Isu-Isl;
    It=Itu-Itl;

    Irst=[Ir; Is; It];

    Ir_z=((1/2)*(Iru+Irl))-((1/6)*((Iru+Irl)+(Isu+Isl)+(Itu+Itl)));
    Is_z=((1/2)*(Isu+Isl))-((1/6)*((Iru+Irl)+(Isu+Isl)+(Itu+Itl)));
    It_z=((1/2)*(Itu+Itl))-((1/6)*((Iru+Irl)+(Isu+Isl)+(Itu+Itl)));

    Irst_z=[Ir_z; Is_z; It_z];

    for j = 1:(N+1)^3

        %---------------Predictive Model-----------%

        %ARM VOLTAGE

        n_ls=Sxy(j,:);
        n_us=zeros(3,1);

        for i=1:3
            n_us(i)=N-n_ls(i);
        end

        Vru = (n_us(1)/N)*(V_C(1) + V_C(2));
        Vrl = (n_ls(1)/N)*(V_C(3) + V_C(4));

        Vsu = (n_us(2)/N)*(V_C(5) + V_C(6));
        Vsl = (n_ls(2)/N)*(V_C(7) + V_C(8));

        Vtu = (n_us(3)/N)*(V_C(9) + V_C(10));
        Vtl = (n_ls(3)/N)*(V_C(11) + V_C(12));

        V_cmv=(1/6)*((Vrl-Vru)+(Vsl-Vsu)+(Vtl-Vtu));

        %Currents

        %Output
        Irst_p(1)= fi_o*Irst(1) + psi_o*(Vrl - Vru - 2*V_cmv -
 2*V_net(1));
        Irst_p(2)= fi_o*Irst(2) + psi_o*(Vsl - Vsu - 2*V_cmv -
 2*V_net(2));
        Irst_p(3)= fi_o*Irst(3) + psi_o*(Vtl - Vtu - 2*V_cmv -
 2*V_net(3));

        %Circulating
        Irst_z_p(1)=psi_z*( ((Vru+Vrl)+(Vsu+Vsl)+(Vtu+Vtl))- 3*(Vru
+Vrl) )+ fi_z * Irst_z(1);
        Irst_z_p(2)=psi_z*( ((Vru+Vrl)+(Vsu+Vsl)+(Vtu+Vtl))- 3*(Vsu
+Vsl) )+ fi_z * Irst_z(2);
        Irst_z_p(3)=psi_z*( ((Vru+Vrl)+(Vsu+Vsl)+(Vtu+Vtl))- 3*(Vtu
+Vtl) )+ fi_z * Irst_z(3);
```

```
        %-----Cost function - MPC Stage I-----%

        cost=y_o*(abs(Irst_ref(1)-Irst_p(1)) + abs(Irst_ref(2) -
 Irst_p(2)) + abs(Irst_ref(3) - Irst_p(3))) + y_z*(abs(Irst_z_ref-
Irst_z_p(1)) +abs(Irst_z_ref - Irst_z_p(2)) + abs(Irst_z_ref -
 Irst_z_p(3)));

        if(aux_cost > cost)
            aux_cost=cost;
            j_opt=j;
            for i=1:3
                Irst_p_opt(i) = Irst_p(i);
                Irst_z_p_opt(i) = Irst_z_p(i);
            end
            U_arms_p=[Vru; Vrl; Vsu; Vsl; Vtu; Vtl];
            V_no=V_cmv;
        end

    end %%% for %%%

    opt_vector=Sxy(j_opt,:);
end
```

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7.7 MPC Stage-II Algorithm Implementation

In the following pages the MPC Stage-II algorithm implementation in a MATLAB/Simulink environment is displayed.

```
function [Gxy, V_C_p] = MPC_Stage_2(opt_vector_e, V_C, I_arms, C, Tsc,
 Vdc)
    %tic

    %-----Gains-----%

    y_d=1;% SM Capacitor Weighting Factor

    %----References----%

    N=2;
    V_C_ref=Vdc/N; %SM Capacitor Voltage Reference

    Gxy = zeros(12,1);

    V_C_p = transpose(zeros(1,12));
    I_C_p = transpose(zeros(1,12));

    n_l=opt_vector_e;
    n_u=N-n_l;

    for i=1:3
        switch i
            case 1
                switch n_u(1)
                    case 0
                        Gxy(1:2)=[0;0];
                    case 1
                        j_opt=0;
                        g_dp=inf;

                        I_C_p(1)=I_arms(1);
                        I_C_p(2)=0;
                        V_C_p(1)= V_C(1)+((Tsc/C)*I_C_p(1));
                        V_C_p(2)= V_C(2)+((Tsc/C)*I_C_p(2));
                        cost=y_d*(abs(V_C_p(1)-
V_C_ref)+abs(V_C_p(2)-V_C_ref));

                        if(g_dp>cost)
                            g_dp=cost;
                            j_opt=1;
                        end

                        I_C_p(1)=0;
                        I_C_p(2)=I_arms(1);
                        V_C_p(1)= V_C(1)+((Tsc/C)*I_C_p(1));
                        V_C_p(2)= V_C(2)+((Tsc/C)*I_C_p(2));
                        cost=y_d*(abs(V_C_p(1)-
V_C_ref)+abs(V_C_p(2)-V_C_ref));
```

```
                    if(g_dp>cost)
                        j_opt=2;
                    end

                    switch j_opt
                        case 1
                            Gxy(1:2)=[1;0];
                        case 2
                            Gxy(1:2)=[0;1];
                    end

                case 2
                    Gxy(1:2)=[1;1];
            end
            switch n_l(1)
                case 0
                    Gxy(3:4)=[0;0];
                case 1
                    j_opt=0;
                    g_dp=inf;

                    I_C_p(3)=I_arms(2);
                    I_C_p(4)=0;
                    V_C_p(3)= V_C(3)+((Tsc/C)*I_C_p(3));
                    V_C_p(4)= V_C(4)+((Tsc/C)*I_C_p(4));
                    cost=y_d*(abs(V_C_p(3)-
V_C_ref)+abs(V_C_p(4)-V_C_ref));

                    if(g_dp>cost)
                        g_dp=cost;
                        j_opt=1;
                    end

                    I_C_p(3)=0;
                    I_C_p(4)=I_arms(2);
                    V_C_p(3)= V_C(3)+((Tsc/C)*I_C_p(3));
                    V_C_p(4)= V_C(4)+((Tsc/C)*I_C_p(4));
                    cost=y_d*(abs(V_C_p(3)-
V_C_ref)+abs(V_C_p(4)-V_C_ref));

                    if(g_dp>cost)
                        j_opt=2;
                    end

                    switch j_opt
                        case 1
                            Gxy(3:4)=[1;0];
                        case 2
                            Gxy(3:4)=[0;1];
                    end

                case 2
                    Gxy(3:4)=[1;1];
            end
```

```
            case 2
                switch n_u(2)
                    case 0
                        Gxy(5:6)=[0;0];
                    case 1
                        j_opt=0;
                        g_dp=inf;

                        I_C_p(5)=I_arms(3);
                        I_C_p(6)=0;
                        V_C_p(5)= V_C(5)+((Tsc/C)*I_C_p(5));
                        V_C_p(6)= V_C(6)+((Tsc/C)*I_C_p(6));
                        cost=y_d*(abs(V_C_p(5)-
V_C_ref)+abs(V_C_p(6)-V_C_ref));

                        if(g_dp>cost)
                            g_dp=cost;
                            j_opt=1;
                        end

                        I_C_p(5)=0;
                        I_C_p(6)=I_arms(3);
                        V_C_p(5)= V_C(5)+((Tsc/C)*I_C_p(5));
                        V_C_p(6)= V_C(6)+((Tsc/C)*I_C_p(6));
                        cost=y_d*(abs(V_C_p(5)-
V_C_ref)+abs(V_C_p(6)-V_C_ref));

                        if(g_dp>cost)
                            j_opt=2;
                        end

                        switch j_opt
                            case 1
                                Gxy(5:6)=[1;0];
                            case 2
                                Gxy(5:6)=[0;1];
                        end

                     case 2
                        Gxy(5:6)=[1;1];
                end
                switch n_l(2)
                    case 0
                        Gxy(7:8)=[0;0];
                    case 1
                        j_opt=0;
                        g_dp=inf;
                        I_C_p(7)=I_arms(4);
                        I_C_p(8)=0;
                        V_C_p(7)= V_C(7)+((Tsc/C)*I_C_p(7));
                        V_C_p(8)= V_C(8)+((Tsc/C)*I_C_p(8));
                        cost=y_d*(abs(V_C_p(7)-
V_C_ref)+abs(V_C_p(8)-V_C_ref));
```

```
                            if(g_dp>cost)
                                g_dp=cost;
                                j_opt=1;
                            end

                            I_C_p(7)=0;
                            I_C_p(8)=I_arms(4);
                            V_C_p(7)= V_C(7)+((Tsc/C)*I_C_p(7));
                            V_C_p(8)= V_C(8)+((Tsc/C)*I_C_p(8));
                            cost=y_d*(abs(V_C_p(7)-
V_C_ref)+abs(V_C_p(8)-V_C_ref));

                            if(g_dp>cost)
                                j_opt=2;
                            end

                            switch j_opt
                                case 1
                                    Gxy(7:8)=[1;0];
                                case 2
                                    Gxy(7:8)=[0;1];
                            end

                        case 2
                            Gxy(7:8)=[1;1];
                    end

                case 3
                    switch n_u(3)
                        case 0
                            Gxy(9:10)=[0;0];
                        case 1
                            j_opt=0;
                            g_dp=inf;

                            I_C_p(9)=I_arms(5);
                            I_C_p(10)=0;
                            V_C_p(9)= V_C(9)+((Tsc/C)*I_C_p(9));
                            V_C_p(10)= V_C(10)+((Tsc/C)*I_C_p(10));
                            cost=y_d*(abs(V_C_p(9)-
V_C_ref)+abs(V_C_p(10)-V_C_ref));

                            if(g_dp>cost)
                                g_dp=cost;
                                j_opt=1;
                            end

                            I_C_p(9)=0;
                            I_C_p(10)=I_arms(5);
                            V_C_p(9)= V_C(9)+((Tsc/C)*I_C_p(9));
                            V_C_p(10)= V_C(10)+((Tsc/C)*I_C_p(10));
                            cost=y_d*(abs(V_C_p(9)-
V_C_ref)+abs(V_C_p(10)-V_C_ref));
```

```
                    if(g_dp>cost)
                        j_opt=2;
                    end

                    switch j_opt
                        case 1
                            Gxy(9:10)=[1;0];
                        case 2
                            Gxy(9:10)=[0;1];
                    end

                case 2
                    Gxy(9:10)=[1;1];
            end

            switch n_l(3)
                case 0
                    Gxy(11:12)=[0;0];
                case 1
                    g_dp=inf;
                    j_opt=0;

                    I_C_p(11)=I_arms(6);
                    I_C_p(12)=0;
                    V_C_p(11)= V_C(11)+((Tsc/C)*I_C_p(11));
                    V_C_p(12)= V_C(12)+((Tsc/C)*I_C_p(12));
                    cost=y_d*(abs(V_C_p(11)-
V_C_ref)+abs(V_C_p(12)-V_C_ref));

                    if(g_dp>cost)
                        g_dp=cost;
                        j_opt=1;
                    end

                    I_C_p(11)=0;
                    I_C_p(12)=I_arms(6);
                    V_C_p(11)= V_C(11)+((Tsc/C)*I_C_p(11));
                    V_C_p(12)= V_C(12)+((Tsc/C)*I_C_p(12));
                    cost=y_d*(abs(V_C_p(11)-
V_C_ref)+abs(V_C_p(12)-V_C_ref));

                    if(g_dp>cost)
                        j_opt=2;
                    end

                    switch j_opt
                        case 1
                            Gxy(11:12)=[1;0];
                        case 2
                            Gxy(11:12)=[0;1];
                    end

                case 2
                    Gxy(11:12)=[1;1];
            end
```

```
            end
        end
        %toc
end
```

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