Fusion Engineering and Design 96–97 (2015) 760–764

Contents lists available at ScienceDirect

Fusion Engineering and Design

journal homepage: www.elsevier.com/locate/fusengdes

Precision Time Protocol support hardware for ATCA control and data acquisition system

Miguel Correia[a,*], Jorge Sousa[a], Bernardo B. Carvalho[a], Bruno Santos[a], Paulo F. Carvalho[a], António P. Rodrigues[a], Álvaro M. Combo[a], Rita C. Pereira[a], Carlos M.B.A. Correia[b], Bruno Gonçalves[a]

[a] Instituto de Plasmas e Fusão Nuclear, Instituto Superior Técnico, Universidade de Lisboa, 1049-001 Lisboa, Portugal
[b] Centro de Instrumentação, Departamento de Física, Universidade de Coimbra, 3004-516 Coimbra, Portugal

HIGHLIGHTS

- ATCA based control and data acquisition subsystem has been developed at IPFN.
- PTP and time stamping were implemented with VHDL and PTP daemon (PTPd) codes.
- The RTM (. . .) provides PTP synchronization with an external GMC.
- The main advantage is that timestamps are generated closer to the Physical Layer at the GMII.
- IPFN's upgrade consistently exhibited jitter values below 25 ns RMS.

ARTICLE INFO

Article history:
Received 1 October 2014
Received in revised form 17 May 2015
Accepted 18 May 2015
Available online 23 June 2015

Keywords:
Synchronization
PTP
Real-time control
ATCA
ITER
Nuclear fusion

ABSTRACT

An in-house, Advanced Telecom Computing Architecture (ATCA) based control and data acquisition (C&DAQ) subsystem has been developed at Instituto de Plasmas e Fusão Nuclear (IPFN), aiming for compliance with the ITER Fast Plant System Controller (FPSC). Timing and synchronization for the ATCA modules connects to ITER Control, Data Access and Communication (CODAC) through the Timing Communication Network (TCN), which uses IEEE 1588-2008 Precision Time Protocol (PTP) to synchronize devices to a Grand Master Clock (GMC). The TCN infrastructure was tested for an RMS jitter under the limit of 50 ns. Therefore, IPFN's hardware, namely the ATCA-PTSW-AMC4 hub-module, which is in charge of timing and synchronization distribution for all subsystem endpoints, shall also perform within this jitter limit. This paper describes a relevant upgrade, applied to the ATCA-PTSW-AMC4 hardware, to comply with these requirements – in particular, the integration of an add-on module "RMC-TMG-1588" on its Rear Transition Module (RTM). This add-on is based on a commercial FPGA-based module from Trenz Electronic, using the ZHAW "PTP VHDL code for timestamping unit and clock", which features clock offset and drift correction and hardware-assisted time stamping. The main advantage is that timestamps are generated closer to the Physical Layer, at the Gigabit Ethernet Media Independent Interface (GMII), avoiding the timing uncertainties accumulated through the upper layers. PTP code and user software run in a MicroBlaze™ soft-core CPU with Linux in the same FPGA, adding programmability and quick implementation of the desired features and upgrades. The paper briefly presents an overview of the ATCA C&DAQ, presenting the PTP and time stamping solution and how it was hardware-implemented, resulting in the RMC-TMG-1588 module. Finally it will describe the synchronization performance tests and results obtained at ITER site as well as indicating further developments to the system, in order to fulfil ITER's requirements.

1. Introduction

Instrumentation for the ITER Fast Plant System Controller (FPSC) was developed by Instituto de Plasmas e Fusão Nuclear (IPFN), contributing with a control and data acquisition (C&DAQ)

* Corresponding author. Tel.: +351 239410108.
E-mail address: miguelfc@ipfn.ist.utl.pt (M. Correia).

http://dx.doi.org/10.1016/j.fusengdes.2015.05.037
0920-3796/

subsystem prototype for fast control applications, founded on the Advanced Telecom Computing Architecture (ATCA) [1,2]. Connection to the ITER Control, Data Access and Communication (CODAC) central system requires timing signals to be synchronized with a Grand Master Clock (GMC), distributed by ITER's Timing Communication Network (TCN), through IEEE 1588-2008 Precision Time Protocol (PTP) [3], with a precision of 50 ns RMS [4]. This paper briefly presents the developed C&DAQ architecture, following a description of the PTP and time stamping mechanism and how the hardware upgrade engineering solutions implement timing and synchronization distribution, achieving compliancy with ITER TCN. Finally, it will address performance tests performed at ITER and present the obtained results.

2. C&DAQ overview

The ATCA C&DAQ shelf contains 14 slots and is equipped with a shelf manager unit, responsible for hardware management [5]. The shelf backplane provides several network topologies with possible redundancy schemes to be configured on the specified ATCA interfaces [6]. Logical slot numbers 1 and 2 are hub-dedicated slots, while the remaining (3–14) are node slots.

The current application uses digitizing units ATCA-IO-PROCESSOR [7] on slots 3 and 5 and a PCI express (PCIe) and timing switch ATCA-PTSW-AMC4 [8] which handles the digitizers' data and timing signals. These in-house developed hardware components belong to the "ITER Catalogue of I&C Products" [9]. Fig. 1 shows the two networks resulting from this setup. The Fabric Interface has a star topology of peer-to-peer PCIe links, between the PCIe switch and endpoints. The Synchronization Clock Interface network distributes the timing signals to all modules in parallel bus topology. A Rear Transition Module (RTM) connects to the Front Board, following draft specifications of PICMG 3.8 "ATCA RTM Zone 3A specification" [10]. The RTM interfaces PCIe data with an external host via cable link [11] and provides PTP synchronization with an external GMC with the inclusion of the RMC-TMG-1588 add-on module, presented in Section 4.1.

3. PTP stack code

PTP and time stamping were implemented with VHDL and PTP daemon (PTPd) codes developed by the Zurich University of Applied Sciences (ZHAW) [13]. This firmware, associated with the adequate hardware assistance, allows to generate sub microsecond precise time stamping. The main advantage is that timestamps are generated closer to the Physical Layer, at the Gigabit Ethernet Media Independent Interface (GMII), avoiding the timing uncertainties accumulated through the upper layers. As shown in Fig. 2, the Message Detection and Time Stamping unit (MD and TSU) intercepts the PTP message Ethernet packets at GMII and generates the corresponding timestamp with the value of PTP Slave clock. The Slave clock is implemented as a PTPv2 time format counter (48-bit word for the seconds and 32-bit word for nanoseconds) where the counter is incremented by an external crystal oscillator (XO) with possible clock frequencies ranging from 50 to 125 MHz. The PTP firmware specifies programmable algorithms for clock drift correction (± 1 ns/2^{30} clock cycles to ± 1 ns/clock cycle) and offset correction (± 1 ns/2^{10} clock cycles to ± 7 ns/2^{30} clock cycles). Lastly, it also features a set of I/O interfaces to perform externally triggered time stamping, output of single and continuous pulse generator, such as Pulse per Second (PPS), and other application-specific functions that may be customized by the user. The reasons for the choice of this IP core were that it supports hardware-assisted time stamping, which benefits its precision. Furthermore it was developed from the manufacturer with successful testing with Xilinx FPGAs, which is a technology already present in our platform and could be quickly incorporated in the current architecture.

4. Hardware implementation

The PTP package was initially tested on a Xilinx SP605 Spartan-6 development kit [14], running in a MicroBlaze™ soft-core CPU with Linux [15], to be subsequently integrated in the existing FPGA of the ATCA-PTSW-AMC4 Front board [16]. However, when porting the SP605 setup to the ATCA platform, it was verified that there was

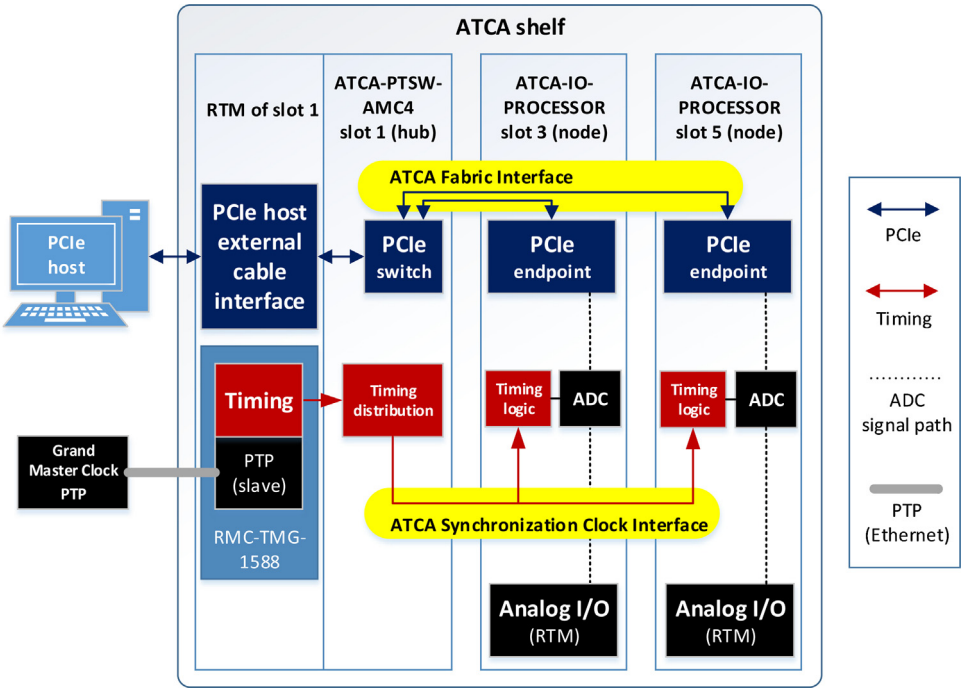

Fig. 1. IPFN's C&DAQ subsystem functional diagram.

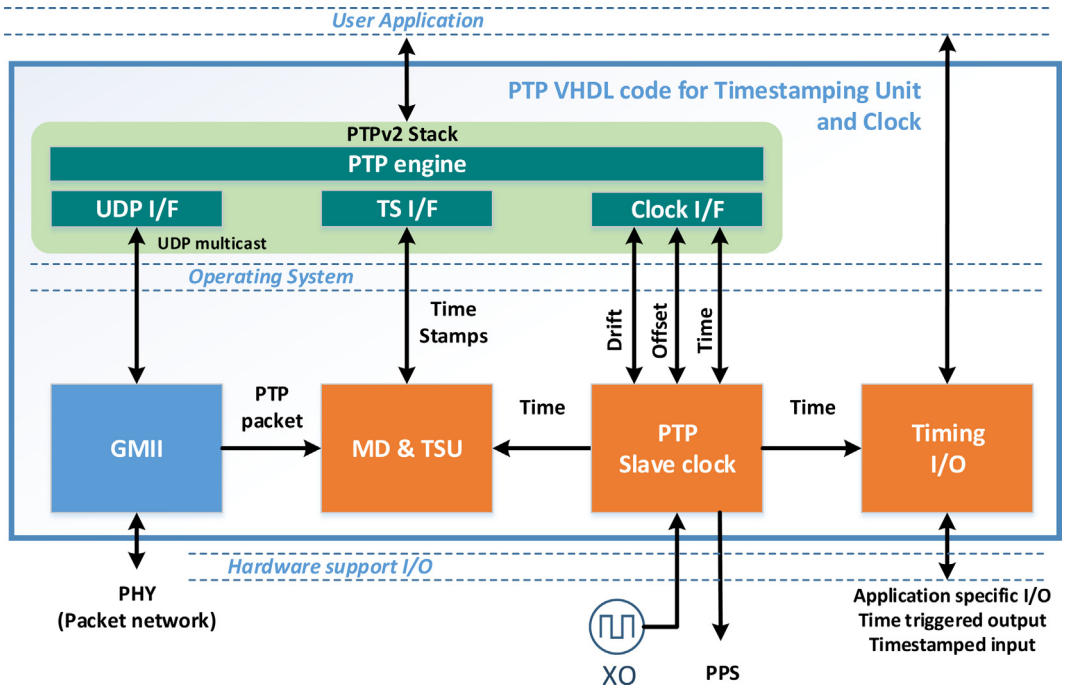

Fig. 2. Functional diagram of the "PTP VHDL code for timestamping unit and clock" firmware, with hardware-assisted time stamping.

not enough onboard RAM in order to run the PTP stack. The solution found was to develop a hardware module, mounted on the RTM.

4.1. RMC-TMG-1588 architecture

The RMC-TMG-1588 is built around the Trenz Gigabee TE-0600 Spartan-6 FPGA-based commercial module, featuring 2 × 128 MB DDR3 SDRAM, 8 MB SPI Flash memory and a Gigabit Ethernet transceiver [17]. With these resources, it is now possible to run Linux and PTP software on the MicroBlaze™ processor. The RMC-TMG-1588 provides connectivity on the RTM panel for easy access (4× LEMO IO, GbE and USB). Fig. 3 shows the RMC-TMG-1588 with TE-0600 mounted on the RTM, showing USB, IO and GbE access on the RTM panel.

The Xilinx Spartan-6 FPGA is the heart of the RMC-TMG-1588 [18], as it implements the PTP code, soft-core OS, external hardware control and IO interface. The PTP VHDL performs packet exchange with the external GMC using the MicroBlaze™/Linux soft processor/OS over GMII, accessing the Physical Layer with a Marvell 88E111 transceiver (PHY) [19], to a RJ45 connector. A 100 MHz XO is provided to increment the PTP clock counter and timestamp generation. IRIG-B timecode [20], 100 MHz clock (CLK) and "pulse per second" signal are encoded from the PTP time output. All three signals (CLK, PPS and IRIG-B) are accessible on the rear panel LEMO connectors and distributed onto the whole C&DAQ subsystem. The RMC-TMG-1588 features an alternative hardware servo loop circuit for PTP clock frequency correction based on the AD9511 [21]. Frequency control is achieved by adjusting local VCXO output through the input control voltage (V_C): (i) internally programmed on the AD9511 charge pump (CP) output, through a low-pass filter (LFP); (ii) firmware controlled by DAC (MAX5202) [22]. Firmware is loaded via JTAG interface or from SPI Flash memory. Additionally, an UART-to-USB bridge (Silicon Labs CP2103) [23], upon device driver install, allows firmware automatic upload and subsequent terminal access to Linux OS. For this purpose, the SPI Flash is mounted with three partitions containing the firmware itself, First Stage Boot Loader and Linux with RAM disc. Fig. 4 summarizes PTP and timing distribution implemented on the TE-0600's FPGA and supporting hardware of the RMC-TMG-1588.

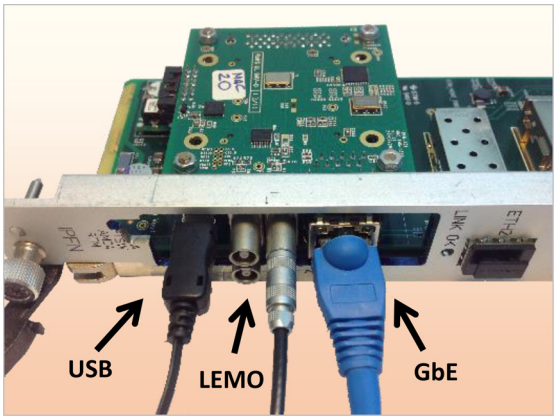

Fig. 3. RMC-TMG-1588 mounted on the ATCA-PTSW-AMC4 RTM, with rear panel connections.

4.2. TCN connection and test setup

IPFN's ATCA C&DAQ subsystem links to ITER CODAC TCN, shown on the bottom of Fig. 4 as a "black box model", where the available connection is the PTP Ethernet link. For jitter measurement, a PPS output of the ITER's Symmetricom Xli GMC unit itself was provided [24]. The test should measure both PPS signals to infer the jitter of IPFN's PPS against the TCN PPS reference, which corresponds to the RMS value of the standard deviation of the skew between both pulses. A LeCroy WaveRunner 620Zi digital oscilloscope was used for signal measurement and to output the necessary mathematical calculations [25].

5. Test

Testing took place at the ITER facilities, where IPFN's C&DAQ subsystem had been previously installed in a dedicated cubicle. An

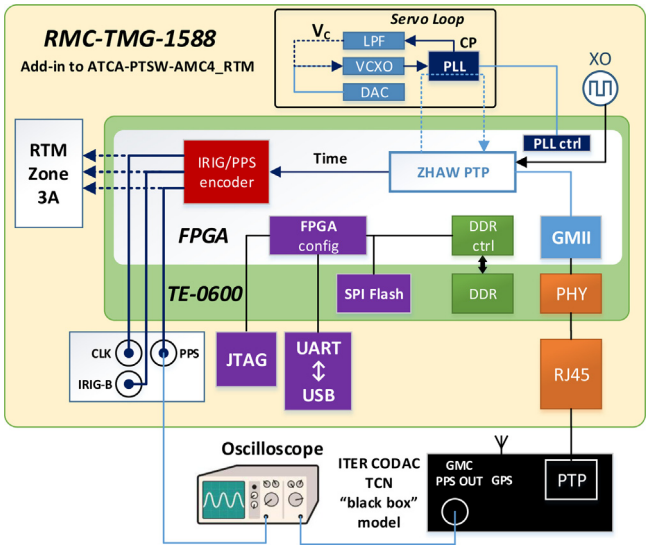

Fig. 4. RMC-TMG-1588 architecture and test setup connecting to TCN.

internal test plan document was previously written and approved by ITER, listing all software installation procedures and performance evaluations. This included the jitter measurement, whose pass/fail criteria threshold had been accordingly set to 50 ns RMS.

5.1. Results

After system bootup and the PTP firmware started running, it took time interval of approximately one minute for both pulse stabilize until both fit within the oscilloscope time span display, set to 1 ms. Once both pulses fit in the display, the oscilloscope was able to start acquiring the skew between pulses over a sufficiently long period (or number of samples) to calculate the jitter. The digital oscilloscope was programmed to automatically output minimum and maximum skew, average skew and skew standard deviation, which is the RMS jitter value. Table 1 is one of the sets of measurements obtained, measuring jitter as 20.94 ns, after almost 30 min (1792 samples @ 1 sample/s). Several sessions took place, with periods of time up to several hours and the jitter measured always remained below 25 ns RMS.

5.2. Issues

Although the pass criteria for timing precision was successfully met, it was verified that the actual average skew wasn't zero, as expected, but a negative value, approximately −158 ns, indicating that the visualized local PPS is advanced by (1 s−158 ns). This is an accuracy issue and it is due to the fact that instead of using the PPS output direct from the PTP code, the PPS used for the tests was computed in the encoding block, using the time output from the PTP, with added processing time. Furthermore this quantity will be slightly different for the several system endpoints, due to the delays caused by different wave propagation paths. A direct software/firmware calibration will be necessary in each system endpoint, in order to cancel this offset.

Table 1
Skew measurements at RMC-TMG-1588, the standard deviation represents the jitter value, which should remain below 50 ns.

Skew measurements	Value
No samples	1792
Minimum	−221.32 ns
Maximum	−99.82 ns
Average	−157.90 ns
Std. deviation	20.94 ns

6. Conclusions

A hardware-assisted implementation of PTP synchronization and time stamping for IPFN's ATCA C&DAQ subsystem was tested, aiming for compliancy with ITER TCN. The main goal of achieving a time precision of 50 ns RMS, was largely surpassed, as IPFN's upgrade consistently exhibited jitter values below 25 ns RMS. Compared to the published results of other implementation for the ITER FPCS [26], IPFN's solution achieved an improved time precision two times higher (corresponding approximately half of the RMS jitter value). One possible reason is that time stamping takes place closer to the Physical Layer (closer to the actual physical clock signal) instead of occurring at the software application layer (farther from the physical clock).

The hardware upgrade was needed, as the former hardware did not allow the desired PTP implementation, due to the lack of SRAM resources. This upgrade is a workaround to this issue, which resulted in the development of an add-on module. The RMC-TMG-1588 benefits from the ATCA-PTSW-AMC4 design, which integrates custom daughter boards mounted on its RTM, providing distribution of clock signals, through the Front Board FPGA, to all system endpoints. This new solution is based on an FPGA commercial module which costs less and reduces hardware development time as the FPGA is electrically setup in the PCB and fully tested, making it easily maintainable and upgradeable.

The add-on hardware architecture may also be quickly adapted to develop other FPGA-based modules, customized for other timing applications and instantly integrated on the hardware platform.

The PLL circuit was not yet used in this particular test, as the goal was achieved by using only the firmware's native clock correction algorithms. The servo loop was designed in the RMC-TMG-1588 because the ZHAW PTP code specifically supports an optional external servo. The RMC-TMG-1588 may act as a multi-purpose timing unit and the AD9511-based circuit adds a wide range of clock generator solutions.

Future work will take care to correct the issue reported in Section 5.2. First by numerically compensating the offset on the current counter scheme and second, by changing the test procedure to use the PPS directly provided by the PTP stack. Further activities also include the integration of additional timing features such as the implementation of a future time events manager. In the current platform, future time events may be programmed and broadcasted by the RMC-TMG-1588 module and stored at the ATCA-IO-PROCESSOR digitizers, which also incorporate FPGAs capable of processing the distributed absolute time to trigger events. In the case of other ATCA compatible endpoints without such capabilities, the ATCA-PTSW-AMC4 front board FPGA is capable of performing the same tasks and associate the sample time information with the endpoint data, available at the corresponding downstream port of the PEX 8696 PCIe switch.

The ATCA Synchronization Clock Interface Multi-point LVDS implementation limits signal frequency to 100 MHz. Alternative interfaces may be needed for higher frequency clocks. IPFN is collaborating with PICMG in developing ATCA specification extensions for Physics, which will allow to improve the current ATCA timing synchronization capabilities.

Acknowledgements

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant

agreement number 633053. IST activities also received financial support from "Fundação para a Ciência e Tecnologia" through project Pest-OE/SADG/LA0010/2013. The views and opinions expressed herein do not necessarily reflect those of the European Commission.

References

[1] PICMG, PICMG® 3.0 Revision 3.0 AdvancedTCA® Base Specification, 2008.
[2] B. Gonçalves, et al., ITER fast plant system controller prototype based on ATCA platform, Fusion Eng. Des. 87 (12) (2012) 2024–2029.
[3] 1588-2008 – IEEE Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems. Available at: http://standards.ieee.org/findstds/standard/1588-008.html
[4] J.-Y. Journeaux, et al., Plant Control Design Handbook (ITER D 27LH2V v7.0), 2013.
[5] A.P. Rodrigues, Intelligent platform management for fast control plant systems, IEEE Trans. Nucl. Sci. 58 (4) (2011) 1733–1737.
[6] M. Correia, et al., *N*+1 redundancy on ATCA instrumentation for nuclear fusion, Fusion Eng. Des. 88 (6–8) (2013) 1418–1422.
[7] A.J.N. Batista, et al., ATCA/AXIe compatible board for fast control and data acquisition in nuclear fusion experiments, Fusion Eng. Des. 87 (12) (2012) 2131–2135.
[8] M. Correia, et al., ATCA-based hardware for control and data acquisition on nuclear fusion fast control plant systems, IEEE Trans. Nucl. Sci. 58 (4) (2011) 1701–1705.
[9] P. Makijarvi, ITER Catalogue of I&C Products – Fast Controllers (ITER D345X28v1.3), 2011.
[10] R. Larsen, High Availability Instrumentation Packaging Standards for the ILC & Detectors. SLAC Publications, SLAC-PUB-12208. Available at: http://www.slac.stanford.edu/cgi-wrap/getdoc/slac-pub-12208.pdf
[11] PCI-SIG, PCI Express External Cabling Specification Revision 1.0, 2007.
[13] IEEE 1588/PTP VHDL Code for Timestamping Unit and Clock. ZHAW. Available at: http://www.ines.zhaw.ch/en/
[14] Spartan-6 FPGA SP605 Evaluation Kit. Xilinx Inc. Available at: http://www.xilinx.com/products/boards-and-kits/EK-S6-SP605-G.htm
[15] MicroBlaze Soft Processor Core. Xilinx Inc. Available at: http://www.xilinx.com/tools/microblaze.htm
[16] M. Correia, et al., Implementation of IEEE-1588 timing and synchronization for ATCA control and data acquisition systems, Fusion Eng. Des. 87 (12) (2012) 2178–2181.
[17] Trenz Electronic TE0600 Series. Trenz Electronic GmbH. Available at: http://www.trenz-electronic.de/products/fpga-boards/trenz-electronic/te0600.html
[18] Spartan-6 FPGA family. Xilinx Inc. Available at: http://www.xilinx.com/products/silicon-devices/fpga/spartan-6/
[19] 88E1111 Product Brief. Marvell Semiconductor, Inc. http://www.marvell.com/transceivers/assets/Marvell-Alaska-Ultra-88E1111-GbE.pdf
[20] IRIG Standard 200-98, IRIG Serial Time Code Formats (1998). Range Commanders Council – Timing Committee Telecommunications and Timing Group. Available at: http://www.irigb.com/pdf/wp-irig-200-98.pdf
[21] AD9511 Clock Distribution IC PLL Core. Analog Devices. Available at: http://www.analog.com/static/imported-files/data_sheets/AD9511.pdf
[22] MAX5200-MAX5203 datasheet. Maxim. Available at: http://datasheets.maxim-ic.com/en/ds/MAX5200-MAX5203.pdf
[23] CP2103. Silicon Labs. Available at: http://www.silabs.com/Support%20Documents/TechnicalDocs/CP2103.pdf
[24] XLi IEEE 1588 Grandmaster Clock (PTPv2). Available at: http://www.microsemi.com/document-portal/doc_view/133460-xli-ieee-1588
[25] WaveRunner® 6 Zi Series. Teledyne LeCroy. Available at: http://cdn.teledynelecroy.com/files/pdf/waverunner_6_zi_datasheet.pdf
[26] D. Sanz, et al., IEEE 1588 clock distribution for FlexRIO devices in PXIe platforms, Fusion Eng. Des. 89 (5) (2014) 652–657.