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A high performance real-time plasma control and event detection DSP based VME system

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Abstract

This paper describes the digital signal processors module of a high performance system, specially designed for real-time plasma control and event detection on the next generation fusion experiments with long duration discharges. The system is composed of a commercial CPU board and several on-site developed intelligent modules inserted in the same VME crate.

Keywords: Event detection; Trigger generation; Real-time digital processing; Parallel processing; Fast control

1. Introduction

Real-time plasma control is an important issue for tokamak advanced scenario operation. Event detection might be a crucial technique for data acquisition on long duration discharges of fusion experiments.

A high performance system, specially designed for real-time plasma control and event detection on the next generation fusion experiments with long duration discharges, has been developed. This system is composed of a commercial CPU board (VME HOST) and several on-site made intelligent modules inserted in the same VME crate. It can operate in stand-alone mode or with the Fast Timing and Event Management System developed by CFN/IST [1]. The VME HOST manages and configures all the modules in the VME crate and provides the interface to the main experiment control and database. The intelligent modules perform data acquisition for real-time processing in order to detect events and trigger the timing system of the data acquisition system of the experiment. They can also perform real-time control and waveform generation.

This paper describes the architecture, hardware and software of the VME intelligent module.

2. Main characteristics and architecture

The module consists of a 6U, A32/D16 VME bus printed circuit board with four independent acquisition, processing and control (APC) channels (Fig. 1) specially designed for data acquisition, real-time parallel processing and control. It

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is an upgrade of another high power processing PCI module developed by the same team [2].

Each APC channel (Fig. 2) is composed of:

- one analogue differential input for data acquisition with 12-bit resolution, ± 5 V voltage range, independent software programmable sampling rate of up to 40 MSPS, and a first in first out (FIFO) memory of up to 32 kword;
- one 32-bit floating point digital signal processor (DSP) (TMS320C44) that can process up to 40 MIPS/80 MFLOPS;
- up to 128 kword 32-bit wide SRAM for DSP program and data;
- one analogue output for control with 14-bit resolution, ± 5 V voltage range, independent software programmable update rate of up to 100 MSPS and a FIFO memory of up to 32 kword.

Data acquisition can be performed in four modes of operation: continuous, post-trigger, pre-trigger, and centred trigger.

The digital to analogue converter (DAC) circuit has two operating modes: control mode and waveform generator. In this last mode the DAC block can generate, in a stand-alone way (without the intervention of the DSP), periodic signals with up to 32 kword per period. The DAC circuit can have an external reference input for hardware multiplying if needed.

The DSPs of all APC channels are synchronised and can directly interchange data among each other for parallel processing thus increasing the processing capacity of the module. The module is cascadable, which means that two DSPs in a module can also directly interchange data with two DSPs in two other modules. This enables the direct interconnection of DSPs of up to two times the maximum number of modules in a VME crate.

In the module there are also up to 16 Mword of 16-bit wide DRAM to keep acquired data. This memory is shared with the VME HOST and may

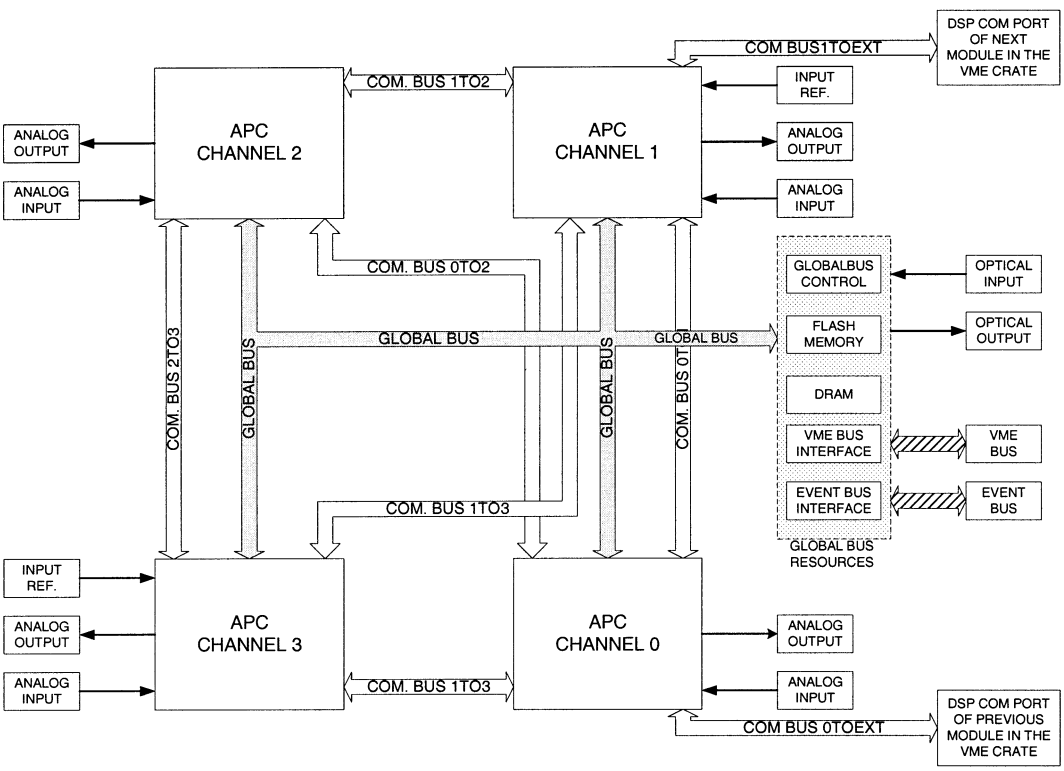

Fig. 1. Architecture of the intelligent module.

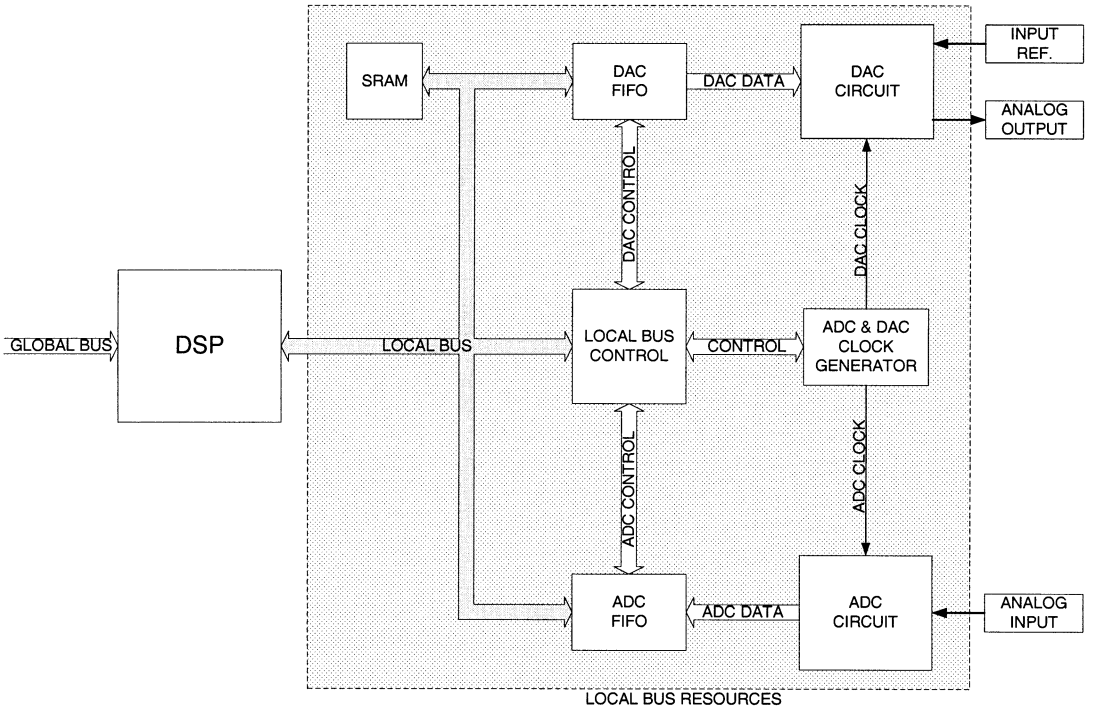

Fig. 2. Architecture of each acquisition, processing and control channel.

be used as a memory buffer between the data acquisition and the VME bus or even to exchange data between DSPs.

In order to have external synchronisation (input trigger) and the ability to trigger other modules (output trigger), the module has a digital input and a digital output, both with optical interface.

One of the most important features of the module is the interface to the Event Bus as a slave (in the VME P2 connector). This bus, designed by CFN/IST [1,3,4], enables the module to send events very fast to the Timing and Event Management System developed by CFN/IST [1,3,4] generating synchronised triggers to the main data acquisition and control system.

The module can generate interrupts to the VME HOST, if needed, and all the configuration of the board, including the VME bus address, is jumperless.

The control and set-up of the module is made by the VME HOST, which sends and receives commands through FIFOs to or from the DSPs.

The digital signal processing algorithms ran by the DSPs, can be downloaded by the VME HOST or can reside in its firmware together with the operating system (OS). This firmware is kept in a flash memory with up to 512KB of memory and is shared by all DSPs. The use of a flash memory to keep the firmware of the module has two great advantages: (i) during power on or reset, the module can start and run an application in a stand alone mode—meaning that it doesn't need the intervention of the VME HOST to download programmes or algorithms; (ii) since the flash memory can be programmed, it is possible to add or change algorithms or programmes to the firmware permanently. It is also possible to keep, in a static way, parameters of an algorithm for later use.

3. The hardware

A 32-bit TMS320C44 DSP from Texas Instruments, which can deliver up to 40 MIPS/80

MFLOPS, is used in each APC channel. Its main function is to process data that has been acquired in the respective analogue to digital converter (ADC) circuit of the APC channel. It also controls the signals that are generated on the DAC circuit of each APC channel and the parameters of acquisition and signal generation such as the sampling rate of the ADC and the update rate of the DAC. A 32-bit 128 kword SRAM is assigned to the DSP for its own operation (data, program and stack purposes) and that is totally independent of the other APC channels (local bus of the DSP) [5].

The acquisition circuit (Fig. 3) of each APC channel is composed of a front end of electronics that conditions the signal to the appropriate voltage range of the ADC and protect it from out of range signals or spikes, an anti-aliasing filter, the 12-bit CLC952 ADC from Comlinear, and a 32 kword FIFO memory. The total independent sampling rate of the acquisition is generated by a software programmable PLL that is controlled by the DSP and a programmable logic device (PLD) MACH211SP from Vantis. The digitised data coming from the ADC is kept in the FIFO memory and can be read by the DSP word by word or using one of the internal DMA channels of the DSP.

The control and waveform generator circuit of each APC channel (Fig. 4) incorporates a 32 kword FIFO memory, a 14-bit HI5741 DAC and an output buffer HA3-5033 that can drive loads of 50 Ω, both from Harris Semiconductor. The update rate of the DAC, as the sampling rate of the acquisition circuit, is also total independent and generated by a software programmable PLL that is controlled by the DSP and the PLD that controls the local bus of each DSP. The DSP writes data only in the FIFO memory, and the PLD controls all the remaining signals needed in order to output the control waveform. The PLD can be configured by the DSP in such a mode that enables the DAC circuit to generate periodic signals with up to 32 kpoint without the intervention of the DSP.

The APC channels 1 and 3 have inputs to implement external hardware multiplying in the DAC circuit.

In order to avoid noise and cross talk between acquisition and control circuits of all APC channels, special attention was given to the design of board layout as well as in the isolation of power sources of the analogue parts of different circuits.

The interface of the module to the VME bus is made with a CY7C960A VME interface controller (VIC) chip and four CY7C964A VME bus driver chips, both from Cypress Semiconductor, and a high density PLD M5-256/120 from Vantis. Those from Cypress Semiconductor where specially designed to make the VME bus interface for any kind of VME transactions very simple to implement. In this slave module the transactions are

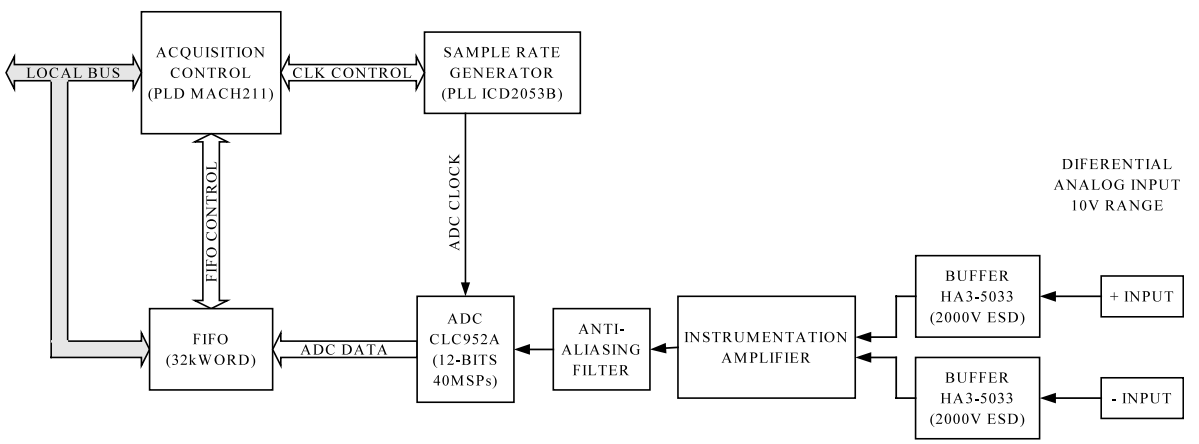

Fig. 3. Data acquisition architecture.

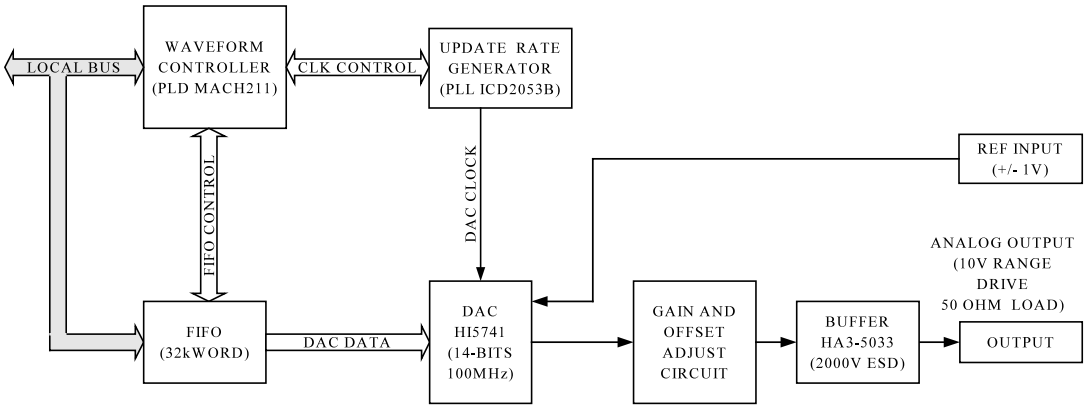

Fig. 4. Control and waveform generator architecture.

A32/D16, the interrupt line 2 is used to interrupt the VME bus HOST and the address initialisation is compliant with the Auto Slot ID utility of the VME64 specification, meaning that may be plug and play.

The VIC has a built-in DRAM refresh controller, which is used to control and refresh up to 4 Mword of 16-bit of DRAM. This DRAM is shared, and can be accessed by the VME bus HOST and all the DSPs. For the VME bus it is in the A32 VME bus address space, for the DSPs it is in the address space of their global bus [5].

In this DSPs global bus address space there are also: two FIFO memories that are used to send and receive commands between the VME bus HOST and the DSPs; the flash memory that contains the OS of the DSPs; an optical digital input; an optical digital output and all the devices that belong to the EVENT bus interface.

In the M5-256/120 PLD is implemented all the decoding logic that is needed to decode all the devices that are in the address space of the global bus of the DSPs, as well as the arbiter that gives the control of the DSPs global bus to each DSP and VME bus HOST.

Each DSP communicates with each other through three of the four high-speed parallel communication ports that they have [5]. The DSPs of APC channels 0 and 1 can also communicate with a DSP in another module in the same crate (Fig. 5).

There are no configuration jumpers on the module. All the hardware configurations or the software that exists in the board can be in system programmed by JTAG interface or under software control.

4. The software

The software of the module is organised in three parts: (i) the OS of each DSP; (ii) the application that each DSP runs; (iii) the drivers that the VME bus HOST application use to communicate with the module.

The OS of each DSP consists in the library functions that give access to all the resources of the module and the kernel that manages the communications between DSPs and the VME bus HOST. This communication consists of commands with parameters that are sent and received through FIFO memories.

The application that each DSP runs may be downloaded from the HOST, or it can be programmed in the flash memory, and consists of a program that calls the OS library functions to access the module resources to get data and processing it in real-time or to generate control signals as needed. Normally, these programs are digital signal processing algorithms such as FFT, IIR, FIR, Convolution, Correlation, Cross-correlation, etc [6].

More complex programs involving more than

one DSP (parallel processing) may be designed when real-time calculations need to be done in less time. Two ways of parallel processing can be designed: (i) more than one DSP process different slices of data of the same signal with the same algorithm at the same time; (ii) more than one DSP process the same data of the same signal with different algorithms at the same time.

When real-time power processing needs to be increased, a signal that is acquired in a APC channel may be distributed to the other DSPs in the same module or in a different modules in the same VME crate, creating this way, a chain of DSPs to real-time parallel processing [5,7].

The software drivers that the VME bus HOST application use to communicate with the module were designed for the OS9 operating system, and for Windows 98/NT OS that runs in embedded PCs VME modules.

5. Conclusion

Laboratory tests have shown that the operation parameters are in good agreement with the design specifications. Very low noise level and almost null cross-talk between the input channels have been achieved.

This system has been used on the ISTTOK operation on alternating plasma current discharges lasting about 200 ms. Results have shown that this DSP-based system is suitable to run an algorithm for real-time control of the horizontal and vertical magnetic fields from the signals provided by a set of magnetic probes.

Three new applications are foreseen in the near future: (i) detection of abrupt changes of some plasma parameters associated with, for instance, internal transport barriers, edge localised modes and disruptions; (ii) joint operation with the IST

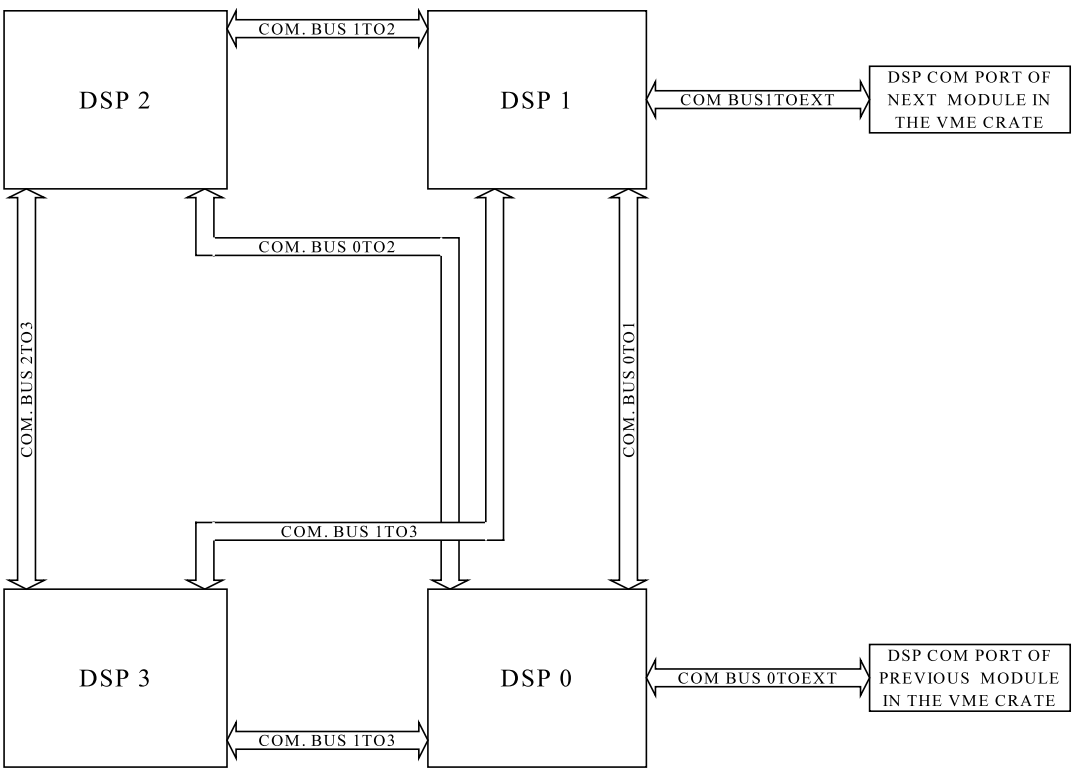

Fig. 5. DSP inter-communications buses structure.

distributed system for fast timing and event management [3] on real-time event-based control in long discharges of magnetic fusion devices; and (iii) control procedures on the TCV device from the results of a pulse height analysis X-ray diagnostic.

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