A 1 GSPS VME Data Acquisition Module

C. F. M. Loureiro, A. M. C. F. Combo, C. M. B. A. Correia
Associação Euratom/IST, Departamento de Física, Universidade de Coimbra, 3000 Coimbra, Portugal

P. Varela, M. E. Manso, C. Varandas, F. Serra
Associação Euratom/IST, Centro de Fusão Nuclear, Instituto Superior Técnico, 1096 Lisboa Codex, Portugal

Abstract

In the following a new data acquisition architecture is proposed allowing high sampling rates along with a large memory data buffer. The modular design allows up to four 250 MHz, 8-bit acquisition channels to operate in an interleaved way, achieving 1 GSPS. Each channel can acquire continuously up to 3 MBytes of data (or 12 MBytes when interleaved). Since several modules can coexist in an acquisition system, provision was made for several parallel operations, including trigger distribution and download of digital signal processing programs.

The module will be used in a dedicated acquisition system for the reflectometry diagnostic on the Asdex-Upgrade tokamak[1].

I. Introduction

The need for faster acquisition rates and the increase in duration of many physical experiments is driving the development of new data acquisition modules with higher sampling rates, sophisticated trigger mechanisms, and large memory buffers. The present work addresses these needs with a new modular architecture that explores the emergence of high speed, high capacity CMOS ICs and the availability of high speed ECL ADCs.

Special attention was given to the fact that new devices with better performance are always emerging, and so the risk for a design to become quickly obsolete is high. This is specially true if the design includes ADCs or digital signal processors (DSPs), as in our case. So we tried as much as possible to separate the ADC's oddities from the data acquisition memory and control. The same is true for the DSP block.

This modular approach resulted in a design with four conceptually different, yet collaborating, parts: a Data Acquisition Block (DAB), a Digital Signal Processor Block (DSPB), a VMEbus interface, and a Common Control Logic (CCL) block (Fig. 1). In the layout phase special care was taken to reflect this organisation in the PCB so that changes on one of these blocks have little effect on the others. This was achieved in part by locating all the CCL and the DAB control logic inside a Xilinx 4010D Gate array.

II. Architecture

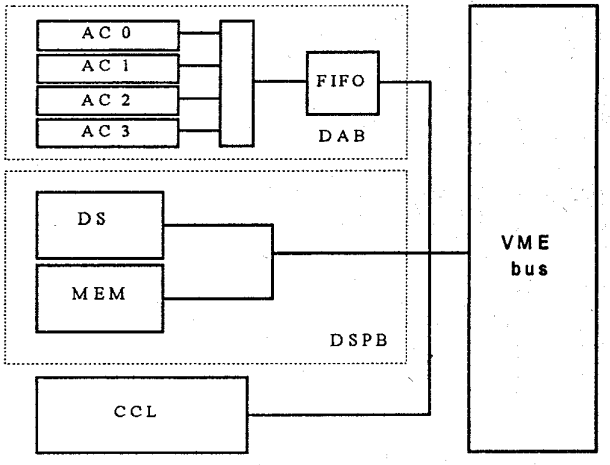

Fig. 1 The general architecture of the module.

A. The Data Acquisition Block (DAB)

The DAB's architecture is depicted in Fig. 2.

The DAB is the heart of our acquisition module. Its operation is usually programmed by writing to a set of registers, and then the user waits for data flowing out of its output FIFOs. This data will be interpreted according to the user progamming of the DAB (number of channels in use, number of words in each acquisition sequence, etc). Essentially the DAB provides logic that is common for all Acquisition Channels (ACs), including acquisition clock generation, trigger and related logic, and memory and output control.

The DAB can operate with up to four ACs in a transparent way. Also its control is independent of the ADC used, which will allow easy upgrading by changing the ADC (minor local redesign needed).

All the control logic and the I/O ports used to program the DAB were made to fit inside a Xilinx 4010D gate array, allowing greater flexibility and big space savings. Also the ECL electronics needed to generate the clock and the fast front-end trigger logic was kept to a minimum.

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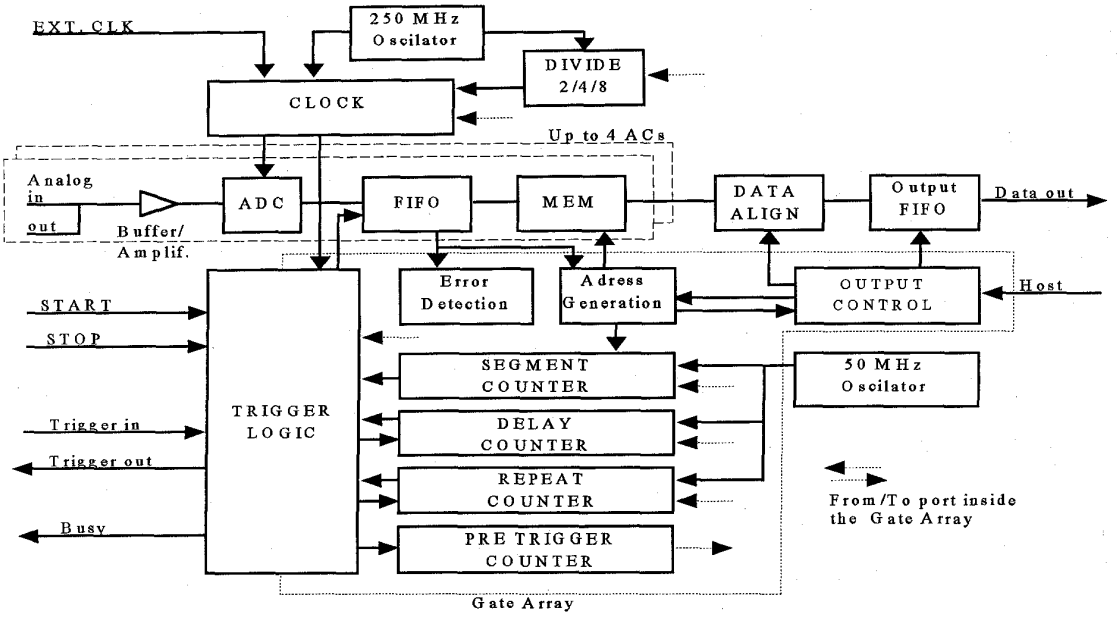

Fig. 2 The DAB's architecture

A.1. The Acquisition Channels (ACs)

Each AC has one 250 MHz 8-bit ADC (Sony CXA1166AK), a circular memory buffer (up to 24 KBytes) constructed using synchronous FIFOs, and a large memory pool (up to 3 MBytes, if 512Kx8 memories are used). The AC may operate with just the circular memory buffer (if the larger memory is not required), helping to tailor the system price to the user needs.

Due to the fast rate of data collection it was necessary to divide the data storage rate by a factor of 5 relative to the acquisition clock so as to be able to use the standard 15 ns static memories. This gave us a 50 MHz clock speed to work with inside the DAB. In fact, due to layout considerations, we opted to divide the acquisition clock by a factor of 6, but keeping the possibility of operating at 50 MHz. This limits our design to ADCs with a data output rate up to 300 MHz, which is well supported by the 100K 300 Series ECL family we use to interface to it. Fortunately the use of the first FIFO memory allows us to work in an asynchronous way relative to the ADC clock. Inside the ACs data is transferred in parallel from the FIFOs to memory.

A.2. Clock

The clock generation circuit allows a choice between an external clock source or the local 250 MHz oscillator. A local programmable port allows also to divide by two, four or eight the frequency of the local 250 MHz oscillator. The chosen clock will be fed to the ADC.

A.3. Trigger

The trigger signal that starts and stops the acquisition of data can be generated from several independent sources. It may arrive from a completely asynchronous external source (START and STOP) or from an internal one under the host VME or local DSP control (by writing to a register).

Bearing in mind that the local DSP or the host VME should be as free as possible for data processing or supervisory control, several advanced trigger features were implemented, usually found only in expensive digital oscilloscopes. These include the PRE-TRIGGER, the SEGMENTED and the REPEAT mode of operation (IV).

There is also provision for a 'clock synchronised' trigger. In this mode the acquisition is done at each clock tick, no further triggering being necessary. This mode of acquisition is to be used with an external clock source generated by the user and allows extreme flexibility: the user may acquire data at any instant, even with changing rates (provided that ADC's minimum time specifications are met).

The Trigger Out signal is to be used in multiple acquisition module systems and allows one module to be the trigger source for all other modules.

A.4. Address Generation

When data acquisition starts and valid data is present in the AC, data from the FIFOs is automatically moved to memory under the control of the DAB output control logic. Meanwhile, if the AC FIFOs are not in danger of becoming full, or if data acquisition is stopped, data will be moved out to the DAB output FIFOs until they become full. This way

data will be available for readout and processing very soon in the acquisition process, and without any concern from the user.

There is the obvious risk of data overflow in the case of very long acquisition times or low readout rates. To minimise this problem, two circular memory pointers were implemented, and it is guaranteed that the read pointer will not pass the write pointer, and that data overwrite will not occur. The Error Detection mechanism will stop the data acquisition in case there is risk of data lost and an interrupt signal may be generated signalling the problem (III.A).

A.5. Output Control Logic

The DAB output control logic is responsible for receiving the data read from the ACs, for ordering it according to the number of ACs in use, and to move it to the DAB's FIFOs. This will be done as soon as data is available and the output FIFOs are not full.

The ordering of the data is needed as internally each AC has a 48-bit bus, and the DAB's outside world was made to have a 32-bit bus for convenient interface either to DSPs or to the VMEbus. As this interface to the outside world is done by reading a FIFO it is also easy to upgrade to different DSPs, or to redesign it for a different bus interface.

A.6. Counters

The different counters in fig. 2 were all designed having in mind a particular mode of operation that will be described later (IV). They are 16-bit counters with the exception of the 40-bit pre-trigger time counter capable of counting at 50 MHz.

B. DSP Block

The DSP block has a TMS320C31 processor with a 0 wait-states interface and up to 2 Mbytes of local memory. This DSP is able to program the DAB and read the data provided by it (maybe using DMA while processing data). It can read the status of the DAB and receive programmable interrupt signals from it (III.B).

The 50 MHz TMS320C31 provides 25 MIPS and 50 MFLOPS for local processing and data reduction.

C. The Common Control Logic (CCL)

The CCL is responsible for managing the interface between the DAB, the DSP block and the VMEbus.

It essentially controls the interface of the local DSP and the host VME to the shared local programming ports of the DAB. It also implements a handshake protocol scheme to allow the host access to the module when the local DSP is present. This is essential as the host will have to download the program the local DSP will run.

Another important task of the CCL is to coordinate the generation of interrupt signals between the DAB and the local DSP or the VMEbus host, or between both the host VME and the DSP.

D. VMEbus Interface

The module implements a VMEbus A32, D32 slave interface with data block transfer capability capable of achieving the maximum 40 MBytes/s transfer rate. The VME host may have complete control of the DAB, which allows the module to operate without the DSP block if desired. In the case this block is present, a Bus Request / Bus Grant scheme was implemented allowing the VME host to control the module local bus. The interface designed supports also a ROAK interrupter capable of generating an interrupt signal using any of the IRQT1-IRQT7 lines.

To speed up some host VME write operations, a special address decode scheme was implemented that allows several boards to be selected simultaneously. This is specially useful in multiple module setups when a trigger signal is to be sent by software simultaneously to several modules (III.B), and when the same program is to be downloaded to all DSPs.

III. Interrupt Structure

In a system designed to operate in real time it is important to have an efficient way to start or interrupt a task or to establish interprocessor communication. So we implemented an interrupt structure allowing for host VME interrupts and for DSP interrupts.

A. DAB Interrupts

The most important interrupt source in the module is the DAB itself. Several interrupts may be generated that completely describe the different states the data acquisition or data transfer can reach. Interrupts can be generated that are related with: trigger signals (START, STOP, TRIGIN); data availability (the state of the DAB's output FIFOs flags, NODATA); error state (NOMEMORY).

The information used to generate these trigger signals is also available through the DAB Status port.

B. DSP Interrupts

The CCL controls all four available interrupt pins of the DSP, and any of those pins may be programmed to receive any of the interrupts sourced by the DAB. Special care was taken so that the particular TMS320C31 interrupt timings are met, and so the DAB's output related triggers can be directly used to generate a TMS320C31 DMA interrupt. This allows the TMS to transfer the acquired data using DMA while doing data processing.

The DSP may also be interrupted by the host VME. The host VME does it by an address-only access to a port, and so

does not need to take control of the module's internal data bus.

C. VMEbus Host Interrupts

The VMEbus host may also be interrupted by the same DAB sources that interrupt the DSP, and also receive interrupt signals sourced by the local DSP. The DSP does it by writing to an appropriate port.

The VMEbus ROAK interrupter implemented can interrupt using any of the VMEbus IRQT1-IRQT7 lines. When appropriate, the status/Interrupt Vector identifying the requester module will be automatically placed in the VMEbus, without the intervention of the local DSP that probably will be working in another job.

IV. Module Operation Modes

The module supports the standard asynchronous START and STOP trigger signals, either from an external source or written by software in a local port.

It also has provision for a PRE-TRIGGER scheme using the AC's FIFO memory with a programmable depth up to 24KBytes. In this mode of operation an initial START signal will be generated, and when desired, a Trigger In signal is sent to signal the end of the pre-trigger time, and then data is moved to memory. The 40-bit Pre-Trigger Time Counter (fig. 2) can then be used to measure the time elapsed between the START and the Trigger In signal. This time counter counts at a 50 MHz rate. It should be noted that using this mode of operation incurs a dead time penalty compared to the trivial START-STOP method (zero dead-time until the AC's memory is full), as the setup of the control logic takes some time to move the pre-sampled data to memory and to reset itself. The dead time will be proportional to the amount of pre-sampled data presamples (bytes) as given by

$$DT_{PT} = \frac{\text{presamples}}{6} * 20 + 350 \quad (ns)$$

as the pre-sampled data must be read at the end of the acquisition cycle and before resetting the control logic (the AC's FIFOs are read in parallel, as explained in I.A.1).

The SEGMENTED mode of operation makes use of the information written to the 16-bit Segment Counter. The Segment Counter will contain the number of words that should be acquired after each START signal. An automatic STOP signal is generated after the specified number of words has been written to the local AC's memory. The DAB's logic automatically resets itself preparing for a new acquisition cycle. The time taken by the DAB's logic to reset itself will be perceived as dead time and in this case will be lower than 200 ns.

The REPEAT mode of operation uses information contained in both the Delay Counter and Repeat Counter (fig. 2). It is helpful whenever it is desired to acquire data a pre-programmed amount of time after the STOP signal. When the STOP signal arrives, the Delay Counter starts counting. When the desired amount of time has elapsed a signal is sent to the Trigger Logic that automatically generates a START signal, and data will be acquired again. This process is repeated until the Repeat Counter reaches the end value. The minimum Delay Counter count time must be bigger than the 200 ns time necessary to re-setup the control logic.

An important point is that the different modes of operation can be mixed together. For instance, PRE-TRIGGER and SEGMENTED can be simultaneously selected to take advantage of the AC's FIFO memory and of the counting of the acquired words and generation of the automatic STOP signal. Another example of mixed functionality would be selecting SEGMENTED and REPEAT. Then, after the first START signal, we would be acquiring a set of 'segmented' data spaced by the delay programmed in the Delay Counter. A final note on mixed modes is that the dead time will then be the maximum of each mode in the mix, and not the sum of the independent dead times.

The BUSY signal (fig. 2) may be used to monitor the availability of the module to new START signals.

V. Application in the Reflectometry Diagnostic in ASDEX Upgrade

The module will be the basis of an upgrade of the dedicated data acquisition system for the reflectometry diagnostic[2] on the Asdex-Upgrade tokamak which is presently using CAMAC based 100/200 MHz modules and VME transputer based 250 MHz modules[3]. The diagnostic operates in the frequency range 16-100 GHz covering densities up to 6.4×10^{19} m^{-3}. The high sampling rates (1GSPS in interleaved mode) provided by this module will allow the acquisition of high frequency reflectometry signals from the higher frequency bands V (50-75 GHz) and W (75-110 GHz). These acquisition rates are required by the need to accurately determine the reflected signal's beat frequency (an error less than 5% corresponds to more than 20 data points/cycle).

VI. Acknowledgements

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VII. References

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